

## ADQ35-WB Datasheet



The ADQ35-WB is a high-end 12-bit dual-channel data acquisition board optimized for high-throughput scientific applications. The ADQ35-WB features:

- One analog channel at up to 10 GSPS included
- Two analog channels at up to 5 GSPS per channel included
- Usable analog bandwidth 9 GHz
- 12 bits resolution
- 14 Gbyte/s sustained data transfer rate to GPU
- 14 Gbyte/s sustained data transfer rate to CPU
- Two external triggers
- General Purpose Input/Output (GPIO)
- Open FPGA for real-time signal processing
- Firmware option for averaging of records
- Firmware option for pulse analysis
- 10-bit data compression for continuous streaming to GPU

## 1 ORDERING INFORMATION

ADQ35-WB is available with a set of options. Follow the procedure to configure the ADQ35-WB. Start with the hardware configurations. The hardware configurations cannot be changed through software commands as they are factory installed.

1. Select the AC-coupled wideband frontend **-WB**. For the DC-coupled analog front-end **-DC**, see 22-2918 ADQ35 datasheet. For dual-gain **-PDRX** analog front-end, see 22-2919 ADQ35-PDRX datasheet.

Select the firmware options. The firmware FWDAQ is always included. Additional firmware options are distributed as firmware image files and can be loaded into the board at any time.

2. Data acquisition firmware **-FWDAQ** is always included.
3. Select one or several of available firmware packages, **-FWATD**, **-FWPD**.
4. Select accessories, open FPGA development kit **DEVDAQ**.
5. Select extended warranty **-WSY**.

The open FPGA is accessed through the design project for each firmware. For **-FWDAQ**, the development kit is **DEVDAQ**. The **DEVDAQ** is a one-time purchase. The FPGA bit files built from the design project can be used on any ADQ35-WB with a valid FWDAQ license (included on all units).

## 2 ADQ35-WB INTRODUCTION

### 2.1 Features

- One and two analog input channels
- 10, 8, or 6 GSPS sampling rates in single channel mode
- 5, 4, or 3 GSPS sampling rate per channel in dual channel mode
- 12 bits resolution
- AC-coupled with usable 120 kHz – 9 GHz bandwidth
- Internal and external clock reference
- Clock reference output
- Internal and external triggers
- 8 Gbyte data memory
- 14 Gbyte/s sustained data streaming to CPU and GPU
- Data format 16-bit MSB aligned or 8 bits compression
- Compression to 10 or 12 bits for streaming to GPU
- Data interface PCIe Gen3 x16
- Averaging firmware FWATD
- Pulse analysis firmware FWPD
- Open FPGA enables custom digital down-conversion firmware

### 2.2 Applications

- Satellite monitoring
- RF IC test
- Radar
- Wireless communication
- Swept-Source Optical Coherence Tomography (SS-OCT)
- LIDAR
- Scientific instruments
- Distributed fiber optic sensing

### 2.3 Advantages

- A compact high-performance digitizer that optimizes the system solution
- Real-time processing and high data throughput
- Teledyne SP Devices' design services are available for fast integration to reduce time-to-market

## **2.4 System design optimization; open FPGA and streaming to CPU and GPU**

High-performance data acquisition systems require high-speed real-time analysis. ADQ35-WB offers a variety of options for efficient system design:

### **Streaming to GPU**

ADQ35-WB supports up to 14 Gbyte/s peer-to-peer streaming and streaming via pinned buffer to GPU. A GPU offers a powerful platform for implementing application-specific signal processing algorithms. Compressing the data to 10 bits allows continuous streaming to GPU for implementation of multi-band receivers.

### **Streaming to CPU**

ADQ35-WB supports up to 14 Gbyte/s to host computer. Implementing the application-specific algorithms in the CPU results in an efficient system.

### **Open FPGA for real-time processing**

ADQ35-WB offers an open FPGA for implementation of the application-specific computations in the FPGA. This gives the most compact system design. Firmware development kit is ordered separately.

### **Digital Down-Conversion**

Digital Down-Conversion (DDC) can be implemented in the open FPGA through the development kit DEVDAQ to reduce the data rate from the ADQ35-WB. This is useful when sending data to a CPU or to a disk. Using the 10-bit compression, all data can be streamed to a GPU and DDC and channelizers can be implemented in the GPU.

### **Usable analog bandwidth**

Even though the traditional -3dB point is at 7 GHz, the frequency band up to 9 GHz has a smooth roll-off. It is thus possible to place the analog signal in this band and adjust the input power to match the attenuation of the ADQ35-WB.

### 3 TECHNICAL DATA

Technical parameters are valid for ADQ35-WB operating with firmware FWDAQ. All parameters are typical unless otherwise noted.

**Table 1 Analog input (front panel A and B)**

Parameter	Condition	Min	Typical	Max	Unit
<b>Basic parameters</b>					
Bandwidth lower	-3 dB		120	500	kHz
Bandwidth upper	-3 dB		7		GHz
Usable bandwidth			9		GHz
Input range			1.4		V <sub>pp</sub>
Input impedance	AC		50		Ω
Input impedance	DC		10		kΩ
Coupling			AC		
Connector type			SMA		
<b>Dynamic performance 2 channels mode at 5 GSPS</b>					
Crosstalk	< 5 GHz		-60		dBFS
Noise power density	0 to 2.5 GHz		-149		dBFS/Hz
SNR	Up to 2 GHz		53.5		dBc
SFDR	Up to 2 GHz		58		dBc
IM3	1.6 GHz, -7 dBFS		-70		dBc
IM3	5.9 GHz, -7 dBFS		-47		dBc
ENOB relative full scale	100MHz, -1 dBFS		8.8		bits
ENOB relative full scale	2 GHz, -1 dBFS		8.5		bits
<b>Dynamic performance, 1 channel mode at 10 GSPS, connector A<sup>1</sup></b>					
Noise power density	0 to 5 GHz		-152		dBFS/Hz
SNR	Up to 2 GHz		53		dBc
SFDR	Up to 2 GHz		58		dBc
IM3	1.6 GHz, -7 dBFS		-70		dBc
IM3	5.9 GHz, -7 dBFS		-47		dBc
ENOB relative full scale	100MHz, -1 dBFS		8.7		bits
ENOB relative full scale	2 GHz, -1 dBFS		8.4		bits

<sup>1</sup> Performance parameters are valid for 1 channel mode using input A. There are no parameters available for 1 channel mode using input connector B.

**Table 2 Clock generator and front panel CLK connector.**

Parameter	Condition	Min	Typical	Max	Unit
<b>Internal clock reference</b>					
Frequency			10		MHz
Accuracy			±3 ±1/year		ppm
<b>Internal sampling clock generator <sup>2</sup></b>					
Frequency range 1	2 channels		5000	5050 <sup>3</sup>	MHz
Frequency range 2	2 channels		4000		MHz
Frequency range 3	2 channels		3000		MHz
Frequency range 1	1 channel		10000	10100 <sup>3</sup>	MHz
Frequency range 2	1 channel		8000		MHz
Frequency range 3	1 channel		6000		MHz
Jitter	10 kHz - 20 MHz		150		fs
<b>External clock reference input (from front panel CLK connector)<sup>4</sup></b>					
Frequency		0.4	10	500	MHz
Frequency <sup>5</sup>	Jitter cleaner enabled	10 -10 ppm	10	500 +10 ppm	MHz
Frequency	Delay line used		10	100	MHz
Delay line tuning range			500		ps
Signal level		0.5		3.3	Vpp
Input impedance	AC		50		Ω
Input impedance	DC		10k		Ω
Input impedance (high) <sup>6</sup>	AC		200		Ω
<b>Clock reference output (on front panel CLK connector)<sup>7</sup></b>					
Frequency			10		MHz
Signal level	Into 50-Ω load		1.2		Vpp
Output impedance	AC		50		Ω
Output impedance	DC		10k		Ω
<b>Physical connector label CLK</b>					
Connector type		SMA			

<sup>2</sup> The internal clock generator can generate frequencies in 3 different ranges.

<sup>3</sup> If the external clock reference deviates from its nominal value, the clock frequency can differ from expected. This is the maximum value where operation can be maintained.

<sup>4</sup> Using a clock reference from an external source to synchronize the ADQ35-WB to the external source.

<sup>5</sup> The jitter cleaner requires the reference frequency to be a multiple of 10 MHz within ± 10ppm.

<sup>6</sup> Software-selectable high-impedance mode.

<sup>7</sup> The internal clock reference of the ADQ35-WB is made available to synchronize external equipment.

**Table 3 Front panel TRIG connector**

Parameter	Condition	Min	Typical	Max	Unit
Connector type		SMA			
<b>Used as input (or GPIO)</b>					
Impedance	DC		50		Ω
Impedance (high) <sup>8</sup>	DC		500		Ω
Signal level	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution <sup>9</sup>	As trigger		50		ps
Update rate <sup>9</sup>	As GPIO			156.25	MHz
<b>Used as output (or GPIO)</b>					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

**Table 4 Front panel SYNC connector (may be used as a trigger source with larger timing grid)**

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
<b>Used as input (or GPIO)</b>					
Impedance	DC		50		Ω
Impedance (high) <sup>8</sup>	DC		500		Ω
Signal range	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution <sup>9</sup>	As trigger		3.2		ns
Update rate <sup>9</sup>	As GPIO			156.25	MHz
<b>Used as output (or GPIO)</b>					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

<sup>8</sup> Software-selectable high-impedance mode.

<sup>9</sup> Timing properties are valid for 5 GSPS in 2 channel mode and 10 GSPS in 1 channel mode. Timing properties scale linearly with sampling frequency.

**Table 5 Front panel GPIO connector**

Parameter	Condition	Min	Typical	Max	Unit
<b>Connector type</b>			SMA		
<b>Used as input</b>					
<b>Impedance</b>			50		Ω
<b>Impedance (high) <sup>8</sup></b>			10		kΩ
<b>Input level high VIH</b>		2			V
<b>Input level low VIL</b>				0.8	V
<b>Update rate <sup>9</sup></b>				156.25	MHz
<b>Used as output</b>					
<b>Output Impedance</b>			50		Ω
<b>Output level high VOH</b>	Into 50-Ω load	1.5			V
<b>Output level high VOH</b>	No load	3.2			V
<b>Output level low VOL</b>	Into 50-Ω load			0.1	V
<b>Output level low VOL</b>	No load			0.1	V
<b>Update rate <sup>9</sup></b>				156.25	MHz

**Table 6 Environment and mechanical parameters**

Parameter	Condition	Min	Typical	Max	Unit
<b>Power and temperature</b>					
<b>Power consumption <sup>10</sup></b>	FWDAQ		48		W
<b>Power supply</b>		10.8	12	13.2	V
<b>Operating temperature</b>	FWDAQ <sup>11</sup>	0		55	°C
<b>Operating temperature</b>	FW options <sup>12</sup>	0		45	°C
<b>Size</b>					
<b>Width 1 slot</b>			18.42		mm
<b>Length</b>			269.55		mm
<b>Height</b>			111.15		mm
<b>Weight</b>			600		g
<b>Compliances</b>					
<b>RoHS3</b>			Yes		
<b>CE</b>			Yes		
<b>FCC</b>	Exclusion according to CFR 47, part 15, paragraph 15.103(c).				

<sup>10</sup> Power consumption depends on firmware option and use case. Power consumption is measured during acquisition and streaming of data at 14 Gbyte/s to PC.

<sup>11</sup> Operating the ADQ35-WB with FWDAQ and streaming data up to 14 GBPS.

<sup>12</sup> Using firmware options from Teledyne SP Devices. Custom firmware designs may result in higher power consumption and thereby lower temperature range.



**Table 7 Custom GPIO expansion. See section 10.**

Parameter	Value
Connector type	40-pin FFC/FPC connector, pitch 0.5 mm
Number of differential IO signals LVDS	8
Number of single-ended IO signals 3.3V	5

**Table 8 Data acquisition**

Parameter	Condition	Min	Typical	Max	Unit
Rearm time <sup>13</sup>				20	ns
Acquisition memory (Data FIFO)	Shared by all channels		8		Gbyte
Record length	2 channels mode in steps of 1	2		2 <sup>32</sup> -1	samples
	1 channel mode in steps of 1	2		2 <sup>32</sup> -1	samples
Pretrigger <sup>14</sup>	2 channels mode in steps of 16	0		16 336	samples
	1 channel mode in steps of 32	0		16 288	samples
Trigger delay <sup>15</sup>	2 channels mode in steps of 16	0		2 <sup>35</sup> -16	samples
	1 channel mode in steps of 32	0		2 <sup>36</sup> -32	samples

**Table 9 Data transfer<sup>16</sup>**

Parameter	Value	Unit
Supported versions of data transfer standard PCIe	Gen1 / Gen2 / Gen3	
Supported number of lanes <sup>17 18</sup>	1 / 4 / 8 / 16	
Data rate to CPU sustained	14	Gbyte/s
Data rate to GPU sustained	14	Gbyte/s
Data rate peer-to-peer to GPU sustained	14	Gbyte/s

<sup>13</sup> Minimum time from the last sample of a record to the next trigger.

<sup>14</sup> Pre-trigger is set by assigning the parameter "horizontal offset" a negative value.

<sup>15</sup> Trigger delay is set by assigning the parameter "horizontal offset" a positive value.

<sup>16</sup> This is the data rate that the ADQ35-WB supports. Other parts of the system may limit the performance.

<sup>17</sup> The ADQ35-WB must be installed in a 16 lanes slot or a slot with a connector with an open end. If a shorter connector is used, the number of lanes and the maximum data rate is limited.

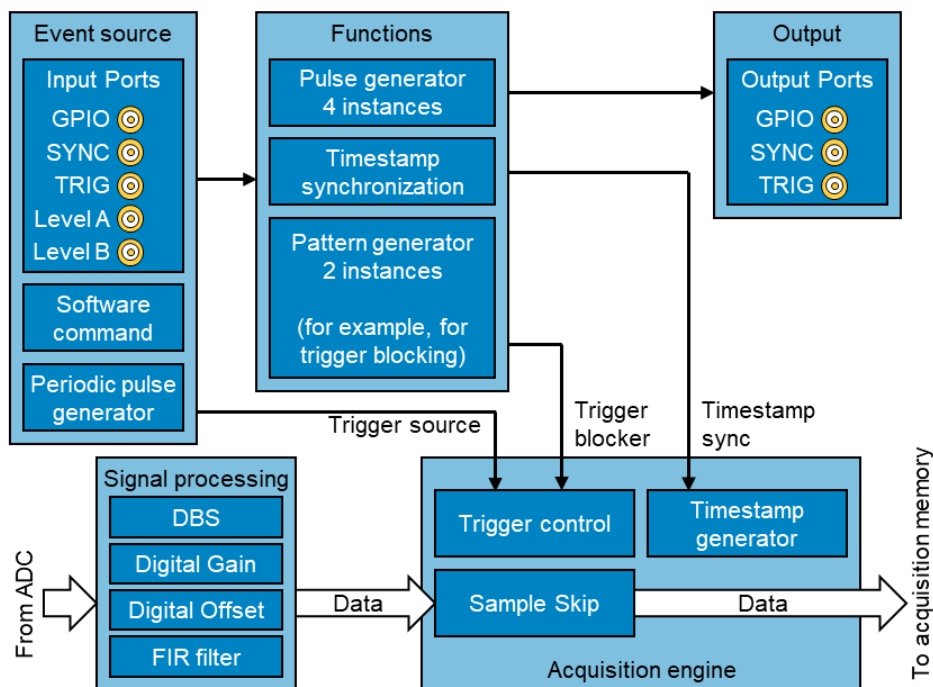
<sup>18</sup> Bifurcation required for 16 lanesSee

**Table 10 Software support**

Parameter	Value
Operating system <sup>19</sup>	Windows / Linux
GUI	Digitizer Studio
Example code	C, Python
API	C / C++
High-level API	LabVIEW / MATLAB / C#

#### 4 FEATURES FOR DATA FLOW CONTROL, SYNCHRONIZATION AND PROCESSING

The ADQ35-WB features an advanced machine for flow control, synchronization, and signal processing. Figure 1 and Figure 2 show the block diagrams. The features are described in the tables below.


**Figure 1 Flow control and synchronization block diagram.**
**Table 11 Digital signal processing blocks**

Object type	Available selections
<b>Digital Signal Processing</b> Included signal processing in the data path for enhanced signal quality.	Digital Baseline Stabilizer (DBS) Digital gain Digital offset Digital FIR filter

<sup>19</sup> See 15-1494 Operating system support for a detailed listing of supported distributions.

**Table 12 Flow control blocks**

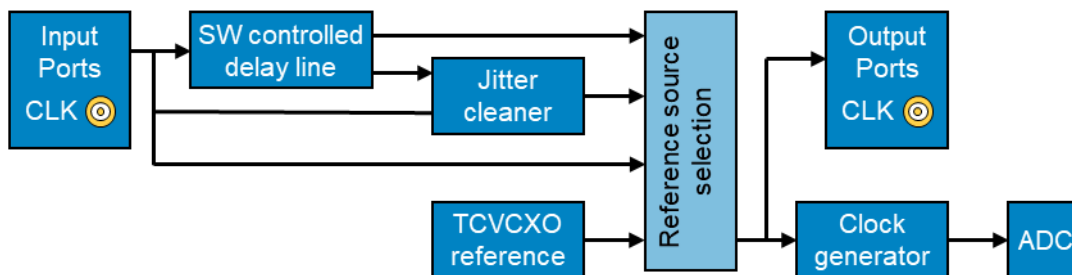
Object type	Available selections
<b>Input ports</b> Electrical connections to the ADQ35-WB for real-time operation (excluding the PCIe data interface) Used as event source.	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference or clock input only) Analog channel A Analog channel B
<b>Event sources</b> Signals for real-time control of activities in the firmware of ADQ35-WB.	Software command External TRIG External SYNC External GPIO Internal periodic event generator Level analog channel A Level analog channel B
<b>Functions</b> Included operations for real-time control of activities in the firmware of ADQ35-WB.	Pattern generator for timestamp synchronization Pattern generator general purpose, 2 instances Pulse generator, 4 instances
<b>Output ports</b> Electrical connections to the ADQ35-WB for real-time operation (excluding the PCIe data interface).	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference output only)

**Table 13 Firmware functions for flow control**

Function	Modes/selections	Event sources as stimuli
<b>Pattern generator for timestamp synchronization</b> Control the time of the ADQ35-WB.		Software command External TRIG External SYNC Internal periodic event generator
<b>Pulse generator</b> Control output pulse shapes. Three instances.	Rising edge Falling edge Pulse length Polarity	Software command External TRIG External SYNC Internal periodic event generator
<b>Pattern generator general purpose</b> For example, used for trigger blocking.	Once Window Gate Trigger counter	Software command External TRIG External SYNC Internal periodic event generator

**Table 14 Firmware functions for acquisition**

Function	Modes	Event Sources as stimuli / control
<b>Trigger</b> Initiate the acquisition of a data record.		Software command External TRIG External SYNC Internal periodic event generator Level analog channel A Level analog channel B
<b>Data acquisition modes</b> Configurations for sending digital data to the host PC.	Fixed record length Dynamic record length (zero suppression)	Selected <b>Trigger</b>
<b>Data transfer modes</b> Transport to CPU / GPU	Streaming with header Streaming without header	User set-up


**Figure 2 Clock generation block diagram.**
**Table 15 Clock generation**

Function	Modes
<b>Clock reference source</b> Phase and frequency reference for the clock system.	Internal External External with jitter cleaner and/or delay line
<b>Sampling clock sources</b> Actual clock for taking the samples of the analog data.	Internal clock generator Direct external clock
<b>Clock output</b>	Selected clock reference

## **5 FIRMWARE**

### **5.1 FWDAQ**

The FWDAQ is included with all digitizers. The firmware includes control of the hardware and recording of data.

The dual-gain channel combination included in FWDAQ requires a separate license for ADQ35-WB.

### **5.2 FWATD**

The FWATD is optional. It includes thresholding for noise suppression and accumulations of waveforms. See datasheet 22-2912 for more details.

### **5.3 FWPD**

The FWPD is optional. It includes detection and analysis of pulses. See datasheet 23-3028 for more details.

### **5.4 Managing firmware**

The digitizer supports multiple firmware images. Note the following about managing firmware images:

- The non-volatile memory on the digitizer can store up to four different firmware images (including the active firmware). Use the tool ADQAssist to change firmware and to upload new images to the digitizer.
- Each hardware can include a license for multiple firmware options. If all firmware images cannot be stored on the device, some may need be stored on the host computer for manual reprogramming via ADQAssist.
- The digitizer (and the enclosing host computer) must be power cycled for the firmware switch to be completed. This is required to let the PCIe bus enumerate with the new firmware.
- Some firmware features require a valid license key to activate. See the ordering information section for details about available firmware features.
- Switching mode between one channel at 10 GSPS and two channels at 5 GSPS requires switching the digitizer firmware image.

## 6 ABSOLUTE MAXIMUM RATINGS

Table 16 Absolute maximum ratings

Parameter	Condition	Min	Max	Unit
<b>Power supply to GND</b>		-0.4	14	V
<b>Operating temperature<sup>20</sup></b>		0	55	°C
<b>Analog in to GND</b>	AC		5	V <sub>RMS</sub>
<b>Analog in to GND</b>	DC	-5	+5	V
<b>TRIG to GND</b>	50-Ω mode	-2	5	V
<b>SYNC to GND</b>	50-Ω mode	-2	5	V
<b>TRIG to GND</b>	500-Ω mode	-2	6	V
<b>SYNC to GND</b>	500-Ω mode	-2	6	V
<b>CLK REF to GND AC amplitude</b>			5	V <sub>pp</sub>
<b>CLK REF to GND DC-level</b>		-5	5	V
<b>GPIO to GND</b>		-1.5	5	V
<b>FFC / FPC differential signal to GND</b>	Powered <sup>21</sup>	-0.5	2.3	V
	Not powered <sup>21</sup>	-0.5	0.5	V
<b>FFC / FPC single-ended signal to GND</b> <sup>21</sup>	Powered <sup>21</sup>	-0.3	3.8	V
	Not powered <sup>21</sup>	-0.3	0.5	V

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the digitizer. The digitizer with PCIe format has a built-in fan to cool the device. The built-in temperature monitoring unit will protect the digitizer from overheating by temporarily shutting down parts of the device in an overheat situation.

The SMA connectors have an expected lifetime of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

<sup>20</sup> The absolute maximum temperature is the range where it is allowed to start the board. The ADQ35-WB has a built-in overheat protection to prevent damage from overheat. The ADQ35-WB may therefore shut down at lower temperature than the absolute maximum. The overheat conditions is depending on the load of the FPGA. For Teledyne SP Devices provided firmware options, see recommended operating conditions in Table 6. For custom firmware the temperature range has to be evaluated from case to case.

<sup>21</sup> The absolute maximum ratings depend on whether the ADQ35-WB is powered or not. It is recommended to use the respective power rail in the FFC connector to power or enable the external drivers to avoid driving overvoltage into an unpowered digitizer. Use the 1.8 V rail for the differential signals and 3.3 V for the single-ended signals.

## 7 TYPICAL PERFORMANCE

### 7.1 Frequency response

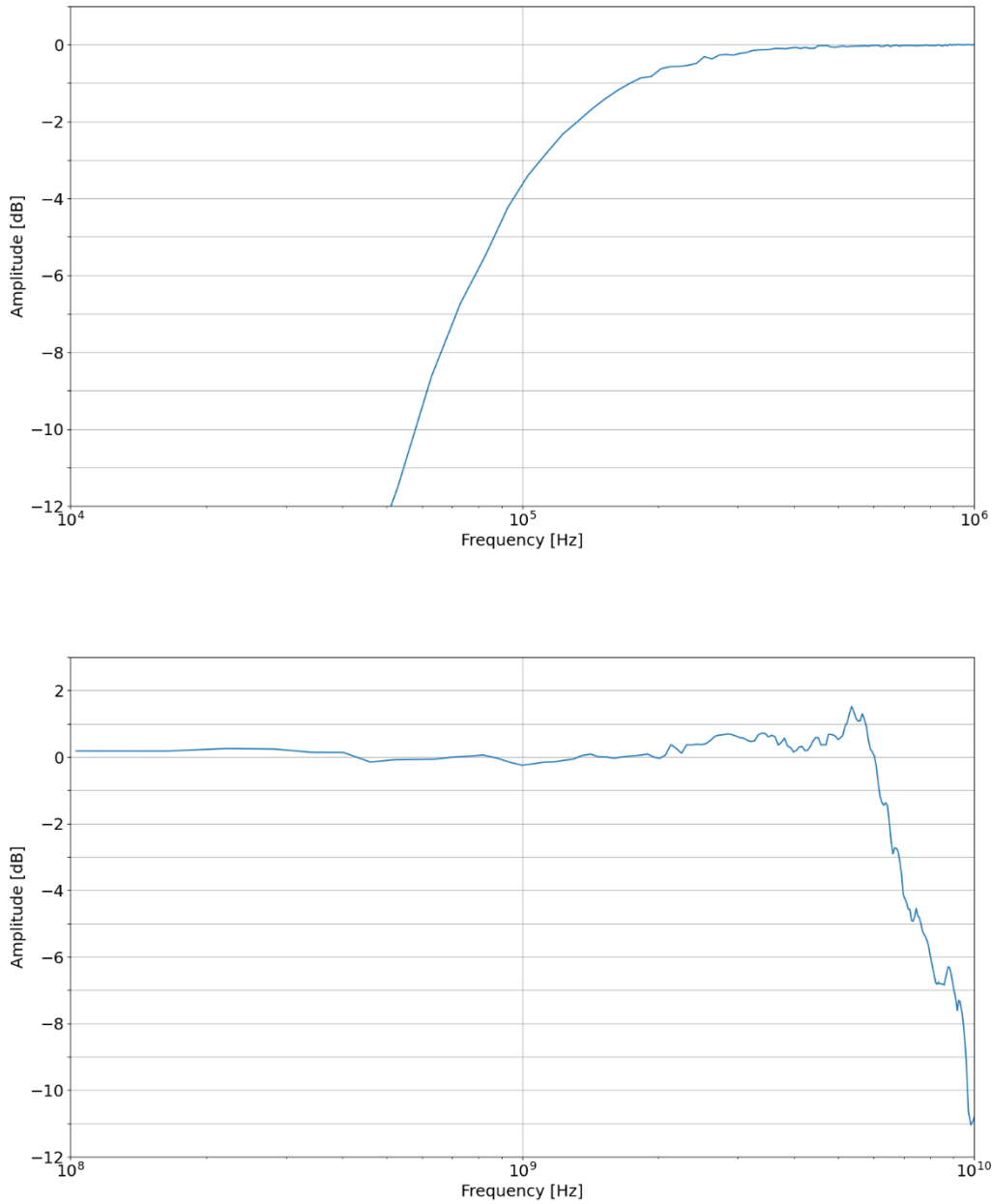
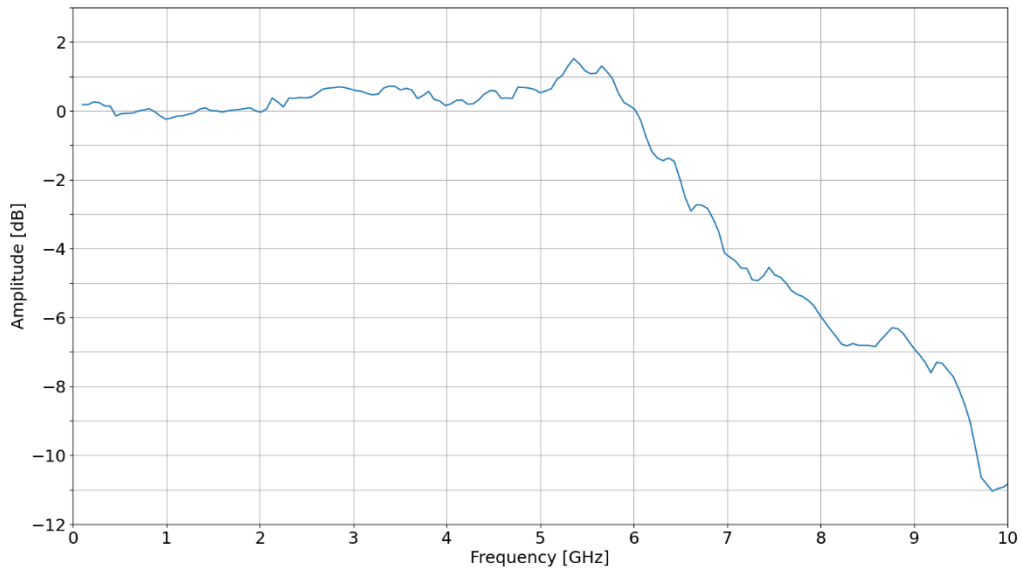
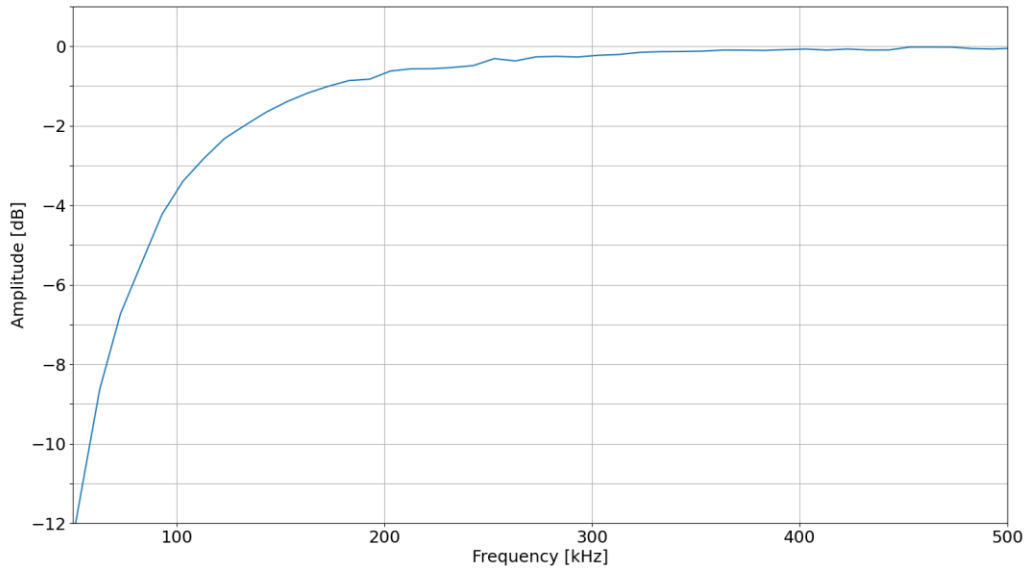
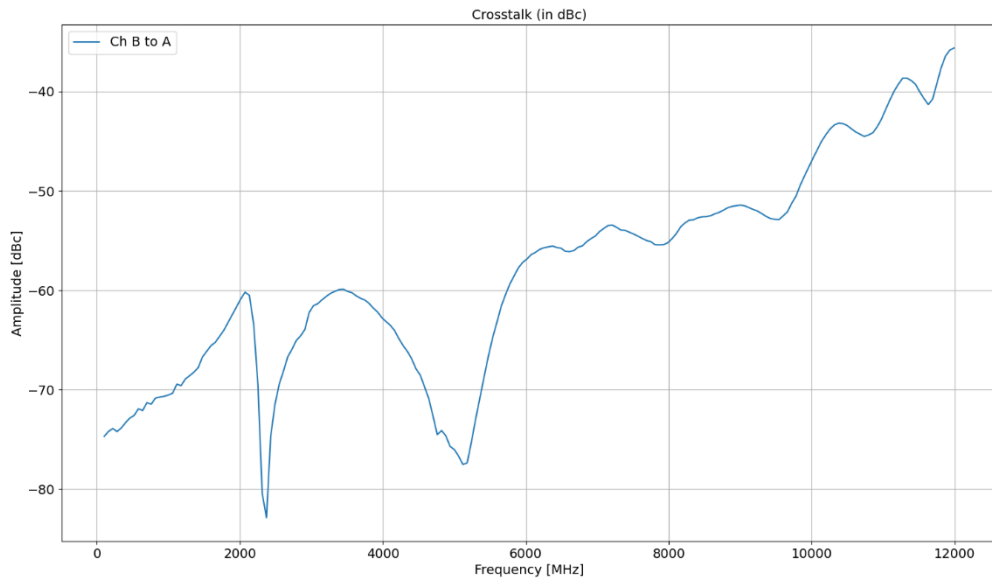


Figure 3 Frequency response, logarithmic frequency scale. 0 dB is nominal input range 1.4 Vpp.



**Figure 4 Frequency response on linear scale. 0 dB is nominal input range 1.4 Vpp.**





**Figure 5 Crosstalk.**

## 7.2 FFT

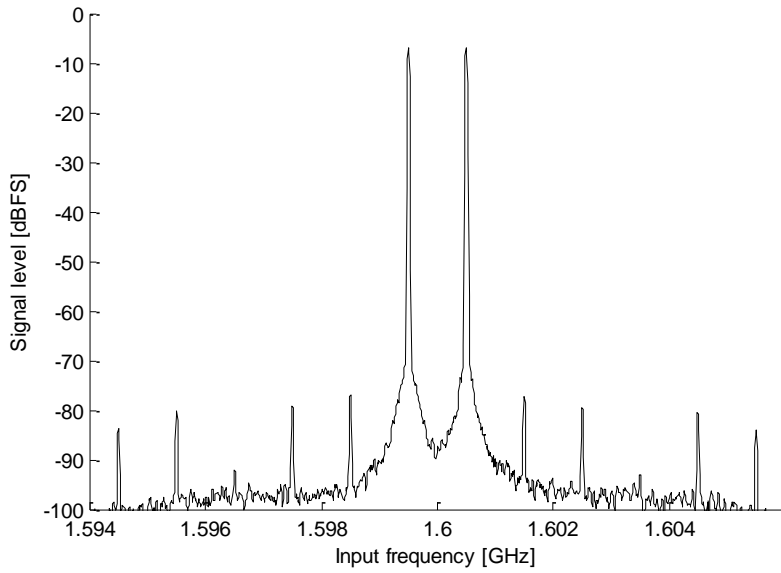


Figure 6 FFT typical two-tone performance at 1.6 GHz.

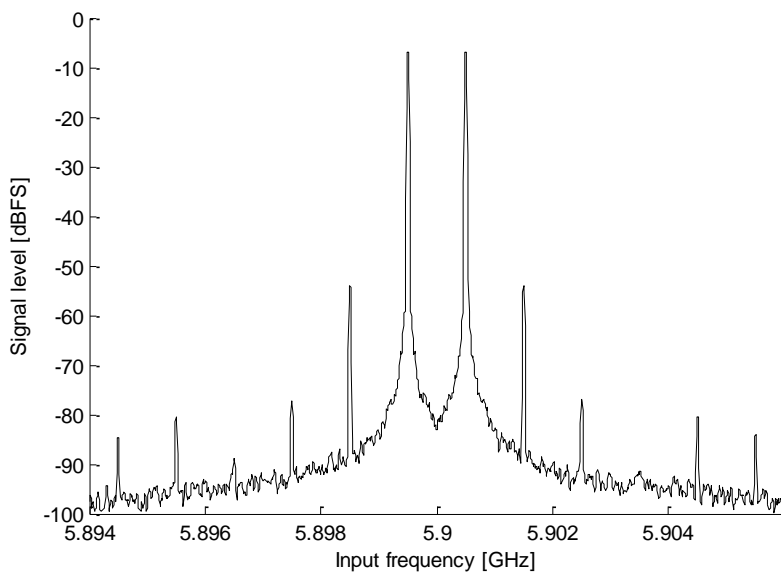
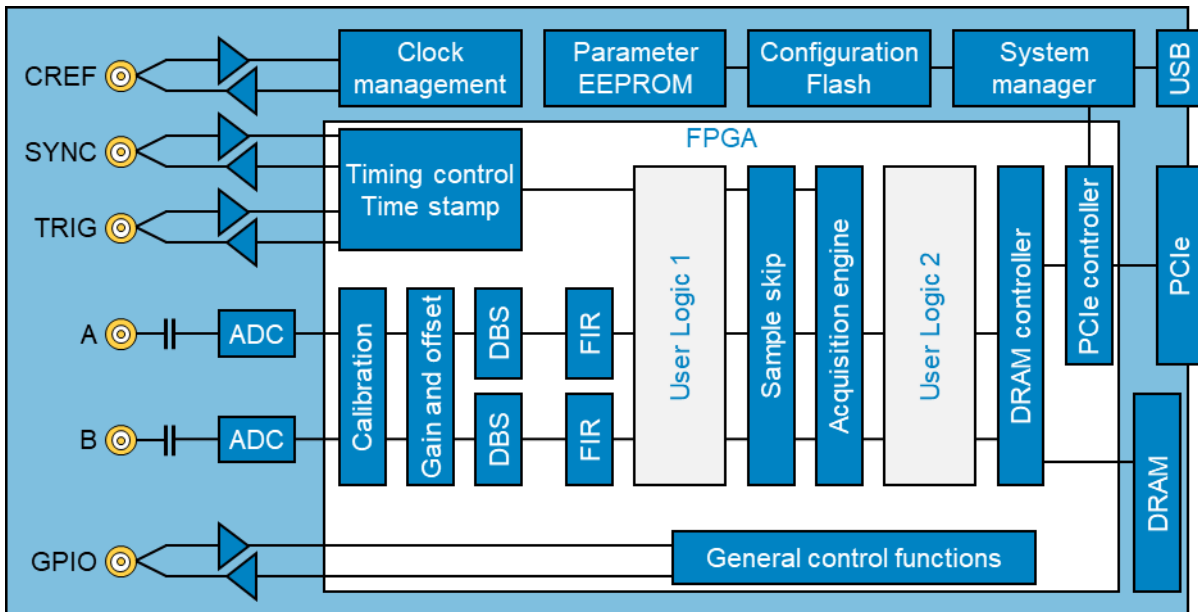


Figure 7 FFT typical two-tone performance at 5.9 GHz.

**8 BLOCK DIAGRAM**



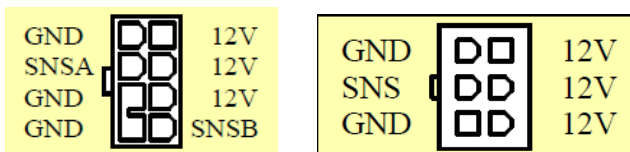
**Figure 8 Block diagram.**

Figure 8 shows a block diagram of ADQ35-WB in 2-channel mode. The boxes “User Logic” are open for custom real-signal processing thought the firmware development kit (purchased separately).

**9 HOST PC INTERFACE PCIE**

The ADQ35-WB-PCIE is powered from the power supply of the PC via a PCI Express 8-pin (2x4) auxiliary power supply connector. The connection in the cable should be as in Figure 9. It is also possible to operate the board from a PCI Express 6-pin (2x3) auxiliary power supply connector. Consider the power ratings for the respective connectors from the PC manufacturer.

It is important that the auxiliary power supply is turned on immediately when the PC starts. Otherwise, the digitizer will not be recognized on the PCI Express bus.



**Figure 9 Power supply connection options. PCB connector.**

## 10 GPIO EXPANSION

The FCP connector allows direct access to the FPGA for building custom expansion boards. The FPC connector requires custom firmware and is accessible through the FPGA development kit. The ADQ35-WB user guide document number 21-2539 contains a description of the connector.

Note that this connector is connected directly to the FPGA. Damage caused by custom hardware failure is not covered by warranty.

Contact Teledyne SP Devices' sales representative for more information.

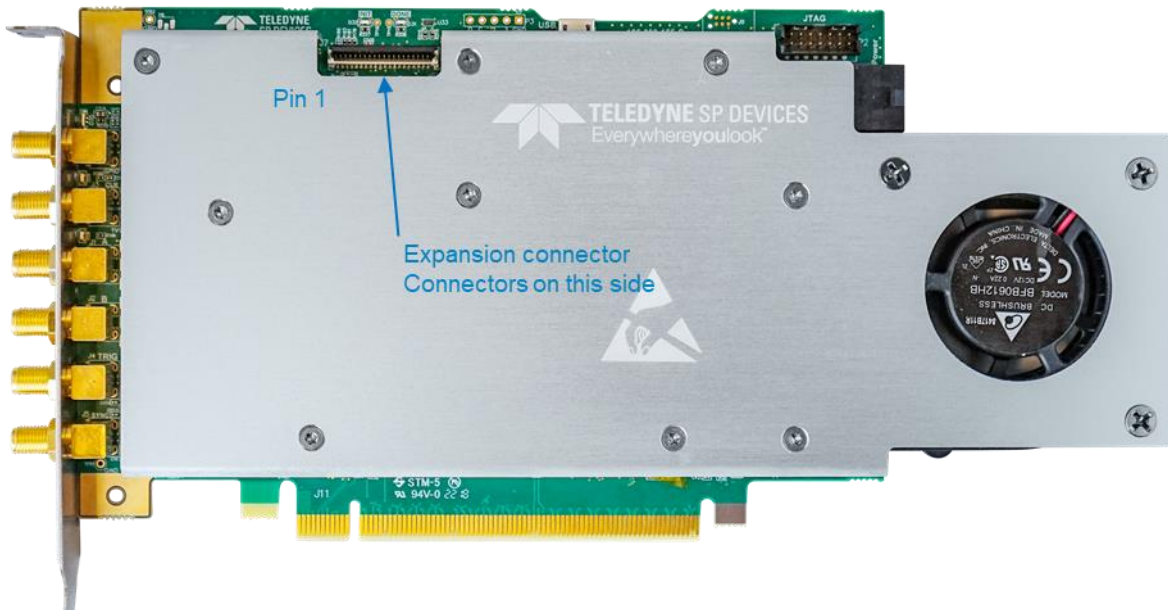


Figure 10 Typical photo showing GPIO expansion connection on the top side.

## 11 MECHANICAL DRAWING

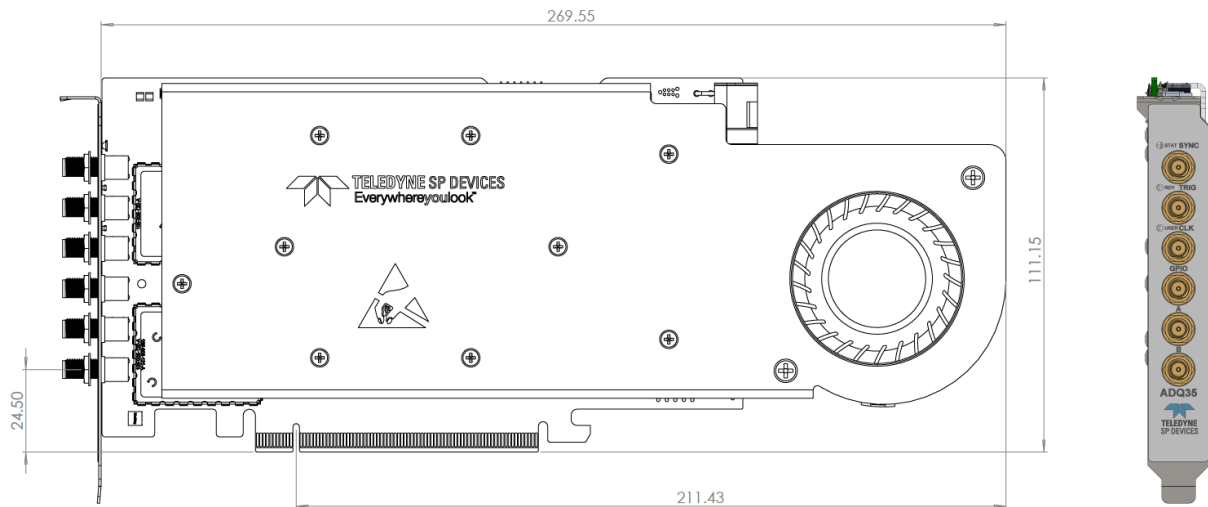


Figure 11 Mechanical drawing.

## 12 REFERENCES

Refer to TSPD's web site [spdevices.com](http://spdevices.com) for the latest version of documents.

15-1494 Supported operating systems

18-2059 ADQUpdater user guide

20-2507 ADQ3 series development kit user guide

20-2521 ADQAssist user guide

21-2539 ADQ3 series user guide

22-2912 ADQ3 FWATD datasheet

22-2918 ADQ35 datasheet

22-2919 ADQ35-PDRX datasheet

23-3028 ADQ3 FWPD datasheet

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