Application Note:

SDR14TX: Synchronization of multiple devices via PXIe backplane triggering

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1 INTRODUCTION

This application note is valid for SDR14 and SDR14TX arbitrary waveform generators (AWG).

This application note describes how to synchronize a multi-channel system of Teledyne SP Devices' arbitrary waveform generators (AWG). An example shows how to build and synchronize an 8-channel AWG system using four SDR14. Method, hardware setup and calibration procedures are described.

Synchronous triggering is accomplished by making the master unit distribute one of its trigger sources (such as the external trigger input) to all other units via the backplane trigger.

2 OVERVIEW

The synchronization contains four steps:

- Use a PXIe chassis and a trigger timing card in the trigger timing slot. The trigger system is based on the PXIe star triggers and the PXIe clock signals.
- Select one AWG as master.
- Run the calibration procedure.
- Select trigger source, for example external trigger, and connect a trigger signal to the master's trigger input. The system is now ready to operate.

The following sections describe the steps in detail.

3 PXIE BACKPLANE TRIGGER SIGNALS

3.1 Overview

The PXIe backplane incorporates high-speed star-routed trigger paths and reference clocks. These are very suitable for use in multi-unit lab setups, in order to trigger and synchronize the units without requiring a large amount of external cables and other equipment. In this document, the PXIe triggering capabilities of the SDR14 and SDR14TX enables multi-channel waveform generator with synchronized triggering.

3.2 Star triggers

A PXIe backplane provides a set of three differential trigger signals, called DSTARA, DSTARB and DSTARC. They are routed in a star-topology from all slots and to all slots via the backplane timing module, and are specified for a slot-to-slot skew of typically less than 150 ps[1]. The DSTARC signal is commonly used to send triggers out from slots, while DSTARA and DSTARB send triggers into slots.

3.3 Clocking

The PXIe backplane signal PXIe_SYNC100 which toggles at a 10 MHz rate, is clocked with the PXIe_CLK100 signal and used to provide a common 10 MHz reference for all AWGs in the PXIe chassis. The CLK100 clock has a specified maximum time skew between any two slots of 200 ps[2].

[1] The skew is a parameter of the selected chassis. See the datasheet of selected chassis for information.
[2] The skew is a parameter of the selected chassis. See the datasheet of selected chassis for information.

4 KEY PARAMETERS IN THE AWG

4.1 Internal clock system

Different AWG models may operate with differing internal clock frequencies. The internal clock frequency is an internal clock used for performing the trigger synchronization. This guide is only applicable when units with the same internal clock frequency are being used. This means that multiple SDR14 or SDR14TX can be synchronized in the same system but it is not possible to synchronize a mix of SDR14 and SDR14TX. The following table contains details of the clock frequencies of each AWG.

AWG	Clock frequency [MHz]	(fs subdiv)	fs [MHz]
SDR14	200	1/4 for ADC 1/8 for DAC	800 for ADC 1600 for DAC
SDR14TX	250	1/8 for DAC	2000 for DAC

4.2 Trigger out and trigger in sampling

An AWG may send out a trigger output pulse via the DSTARC output. This output will be synchronous to the internal sample clock of the AWG. Any AWG that receives this trigger pulse via its DSTARB input will then sample the trigger pulse with its own phase-locked sample clock. The trigger signal will experience some routing delay through the PCB, backplane, timing module and FPGA.

In the current implementation of the trigger sampling logic, the trigger input is sampled twice per internal clock period, which gives the following trigger precision:

AWG	Clock frequency [MHz]	Trigger precision [MSPS]
SDR14	200	400
SDR14TX	250	500

On its own, this is not enough to achieve synchronized triggering since the trigger sampling rates are all lower than the sampling frequencies of the AWG. However, since the AWGs are all phase-locked to the same backplane reference, the internal clocks of the separate AWGs will be aligned in phase. Therefore, since the trigger points out a specific clock period, the trigger will be aligned with sample precision for all the AWGs.

4.3 Calibration of synchronization triggers

If deterministic triggering of the boards is to be accomplished, it is important that no setup/hold violations exist in the trigger sampling. If the routing delay of the trigger signal is causing the trigger edge to be directly aligned with the rising edge of the clock this will result in an uncertainty with regards to which clock cycle the trigger is asserted on.

Because of this, the firmware provides a means of controlling the DSTARB input delay via the AWG application programming interface (ADQAPI). This delay is adjustable in steps of 78 ps, between 0 to 2.4 ns. This can be calibrated for a specific system and stored in the EEPROM of the device. The saved delay setting will then automatically be loaded each time the device is started.

Note! The calibration can be done at Teledyne SP Devices at delivery of the system. Example code with delay calibration can be provided upon request. The calibration procedure software is available for MATLAB only. Contact a Teledyne SP Devices' sales representative for guidance on delay calibration.

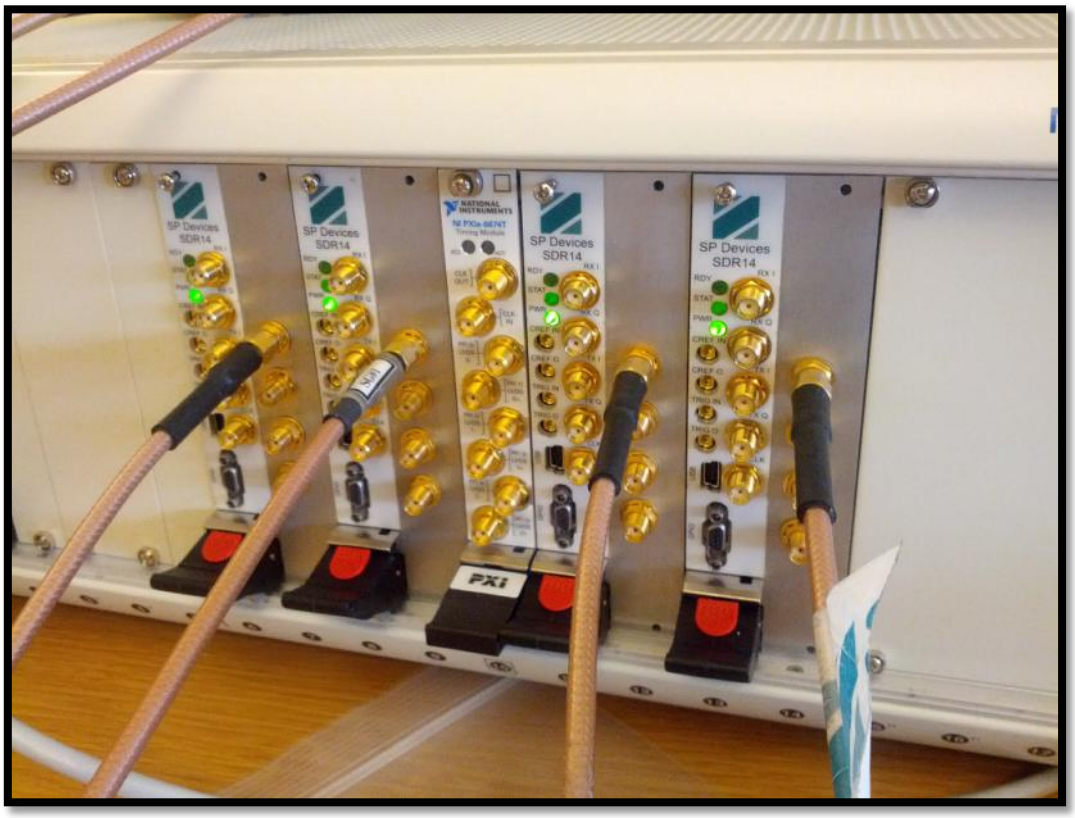
5 USING THE SYSTEM

Operation is started by selecting a trigger source, e.g. level trigger, software command, or external trigger in the master AWG. When triggered with the selected type, the trigger is distributed via star-triggers in the backplane and all cards are triggered simultaneously.

6 EXAMPLE USE CASE – 8-CHANNEL WAVEFORM GENERATION WITH SYNCHRONIZED SEGMENT SWITCHING

6.1 Equipment

NI PXIe-1075	x1	Chassis
NI PXIe-6674T	x1	Timing Module
NI PXIe-8105	x1	Embedded Controller
SDR14	x4	AWG



6.2 Use case

The desired functionality of the lab setup in this use case is a multi-channel waveform generator. The SDR14 is used, which has two analog inputs and two analog outputs per unit. Four of these units

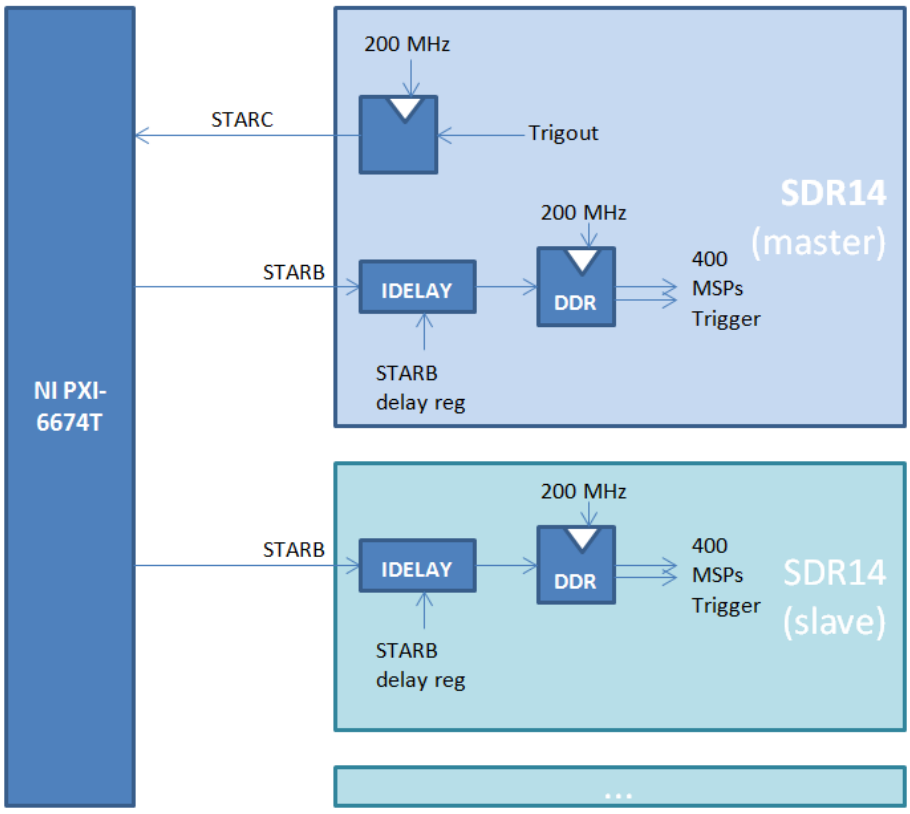
have been inserted in to a PXIe chassis, and the goal is to use these together to create a synchronized eight-channel waveform generator.

One board is designated as the master unit, sends a trigger to all boards, including itself. Upon receiving the trigger signal, all boards start transmitting their pre-programmed waveform data. This occurs synchronously between the boards, with all the board sample clocks locked to the backplane clock reference, and all boards having a deterministic delay from trigger to output, which does not change between system startups.

The triggering is done through the timing module, in the following way:

(Master SDR14) → DSTARC → Timing module → DSTARB → (all SDR14 units).

A block diagram of the triggering is shown below:



This setup has been verified to have deterministic relative phase between the output waveforms across multiple startups and is already successfully used in customer applications.