Application note

Introduction to setting up PDRX

Table of Content

1 DOCUMENT OVERVIEW

1.1 Scope

This application note is an introduction to how to set up the ADQ digitizer for pulse data measurements. The system assumes to be using dual-gain amplifier. A dual-gain design is based on multiple signal paths with different gain, one high-gain path for weak pulses one low-gain path for large pulses. The application note is based on the digitizer with integrated dual-gain amplifier, ADQ3-PDRX, Figure 1. PDRX stands for Pulse Dynamic Range eXtension. The application note can also be applied to systems using a dual channel digitizer and a custom external dual-gain amplifier.[1]

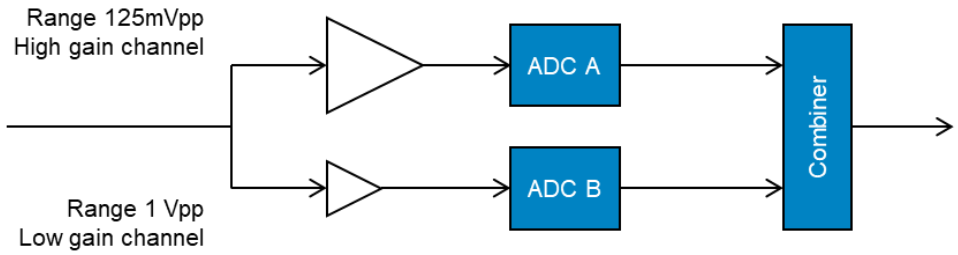

Figure 1 Illustration of the dual-gain amplifier concept. The signal ranges mentioned are used on ADQ32-PDRX hardware.

1.2 Test case

The measurement situation when a dual-gain digitizer gives an advantage is when detecting unipolar pulses. The signals coming into the system contains large and small pulses. The core of the application is to determine the amplitude ratio between pulses and their respective timing.

- The timing accuracy is primarily related to the sampling rate of the digitizer, so we use an ADQ32, which is sampling at 2.5 GSamples/s.
- The accuracy of the amplitude ratio is primarily related to the dynamic range of the digitizer, so we use the version ADQ32-PDRX, which has a built-in dual-gain amplifier.

1.3 Relevant features of the digitizer

The following features are used in this application note:

- The set-up will benefit from the full range of the digitizer by applying DC-offset

[1] This application note assumes knowledge about dual-gain pulse recording applications. An introduction to the concept of dual-gain is available at https://www.spdevices.com/what-we-do/technology/pdrx

The on-demand webinar also describes the dual-gain in detail https://www.spdevices.com/en-us/Events_/Pages/Webinar-Digitizer-with-integrated-dual-gain-amplifier-for-maximizing-dynamic-range-in-pulse-measurements.aspx

- Correcting baseline with DBS (Digital Baseline Stabilizer) for a precise baseline. This enables accurate threshold operation for triggering or pulse detection. DBS also suppresses interleaving pattern noise (for interleaved digitizers).
- Increase the ratio (dynamic range) by combining high gain and low gain channels. This consist of an analog dual-gain amplifier front-end and a digital channel combination.

1.4 Supported digitizer models

The ADQ3-PDRX is an implementation of a dual-gain amplifier directly on an ADQ digitizer. The application note is valid on the ADQ-PDRX hardware. It can also be applied to any ADQ3-series digitizer with 2 inputs that are connected to an external dual-gain amplifier.

The application note is produced using software and firmware release 2023.3.

The digitizer hardware models used in the tests are ADQ32-PDRX with datasheet 23-2797-D and ADQ32 with datasheet 20-2378-G.

2 INPUT SIGNAL

(How the test signals are generated is described in the is described in section 11. Note that the test signals are not designed for demonstrating signal quality. These signals are designed to illustrate features only. Refer to the datasheet for performance metrics.)

The input signal in this test is a large pulse followed by a weak pulse. The pulses are 3.2 ns square wave shaped. The pulses have positive polarity, but all discussions are equivalent for negative pulses. The upper plot in Figure 2 shows a large pulse. The weak pulse is hardly visible for the eye in the plot, so the lower part zooms in on the weak pulse.

These plots are the result from dual-gain amplifiers, DC-offset, DBS and channel combination. The following sections will show how this is set up.

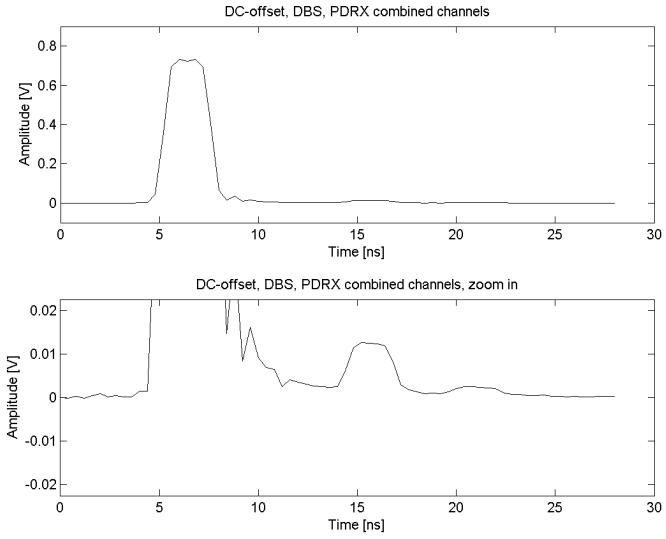

Figure 2 Illustration of the test signal containing two pulses with different amplitude. The upper part shows the large pulse. The lower plot is zoom-in on the small pulse. DC-offset, DBS, and channel combination applied.

3 DC-OFFSET

The ADQ3 digitizer has a symmetrical input signal range. For unipolar pulses, half of the dynamic range is lost. The test signal of Figure 2 is applied. Figure 3 shows the two outputs from the dual gain amplifier digitized by the two ADCs of ADQ32-PDRX. The upper red curve is the low-gain channel with 1Vpp range, and the lower blue curve is the high-gain channel with 125 mVpp range. In Figure 3 it is seen that the large pulse is cut by overrange in the ADCs in both channels. It is also seen that the lower half of digitizer's signal range is not used.

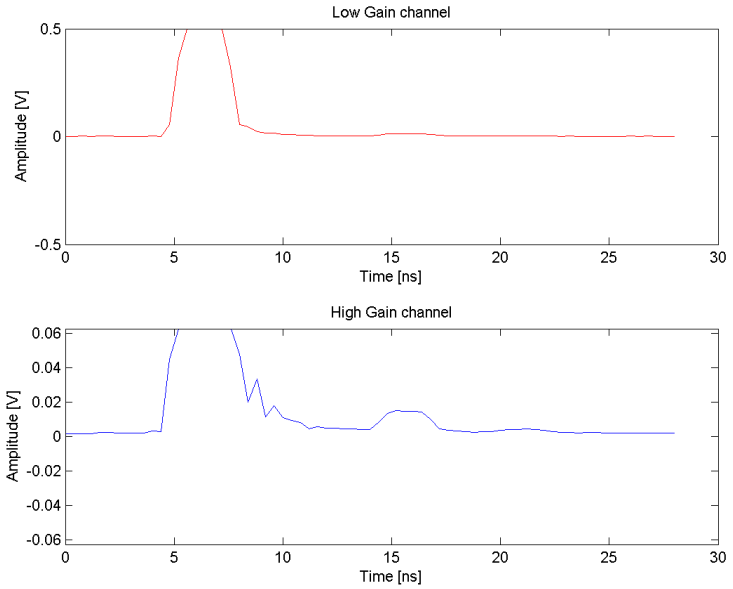

Figure 3 Data from separate high-gain and low-gain channels. There is overrange from the large pulse while half the signal range is unutilized in both channels.

To use the ADQ3 with unipolar pulses a DC-offset can be applied. The DC-offset moves the signal range of the digitizer to the positive or negative polarity. In Figure 4, the DC-offset moves the signal range to the positive half. The signal is no longer cut by overrange in the upper Low-gain channel (red curve). The low-gain channel can be used for detecting the large pulses. The high-gain channel (bottom blue curve) cannot be used for large pulses, but the small pulse is clearly visible.

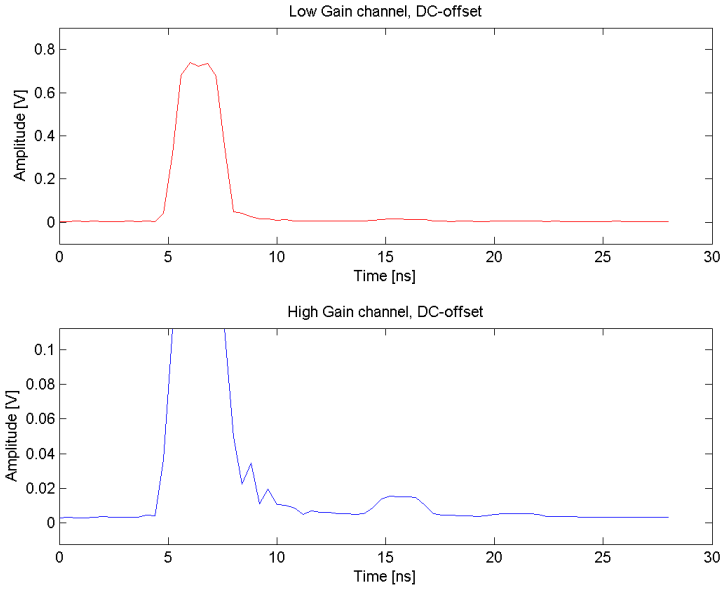

Figure 4 Separate channels with DC-offset applied. The full signal range is used, and the large pulse is no longer cut in the low-gain branch.

The block diagram of the ADQ32-PDRX including DC-offset is in Figure 5. The DC-offset has several properties:

- The DC-offset is added to the signal in the analog domain and is thus given in [mV] and the level relates to the range of the input signal.
  - Notice that the analog range of the different branches are different.
  - The range of the low-gain branch is 1 Vpp so, for example, setting DC-offset to +/-400mV result in +/-90% offset
  - The range of the high-gain branch is 125 mVpp so, for example, setting DC-offset to +/-50mV result in +/-90% offset.
- The DC-offset is added the analog signal and does not leak to the input.
  - The DC level seen at the input is not changed.
  - The signal range of the ADC component is still symmetric. The DC-offset moves the input signal up or down relative to the signal range of the ADC component.
  - A positive DC-offset is used for negative pulses
  - A negative DC-offset is used for positive pulses
- The code range out from the ADC components are the same regardless of the analog signal range. (see 21-2539 ADQ3 user guide for conversion between volts and codes)
  - Setting low-gain channel DC-offset to +/-400mV result in low-gain code level +/-26214 for 0V input signal. [2]

[2] Digital code range is from -2^{15} to $2^{15}-1$ = –32768 to 32767. The analog signal range is from –500mV to +500mV so a DC-offset of –400 mV corresponds to 400/500 * -2^{15} = –26214.

- Setting high-gain channel DC-offset to +/-50mV result in high-gain code level +/-26214 for 0V input signal.
- The digital numbers from the digitizer remains from (-2^{15}) to (2^{15}-1). The position of the analog input zero level is shifted by the DC-offset and is not anymore represented by digital code 0.
- Applying DC-offset means that the natural translation of analog signal level 0V to digital code 0 is no longer valid.

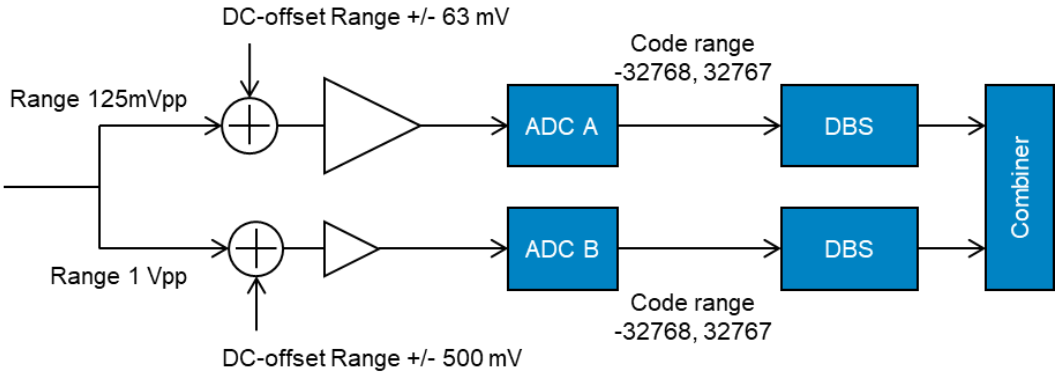

Figure 5 Block diagram for DC-offset and DBS in ADQ32-PDRX.

The DC-offset can be set close to the boundaries of the signal range. It is not recommended to set the DC-offset too aggressive. Then overshoot can be clipped, and the system then becomes non-linear, which may introduce problems if filters are applied. Also, setting baseline outside the range is not recommended since the digital baseline stabilizer (DBS, see section 4) will not work.

4 DIGITAL BASELINE STABILIZER, DBS

4.1 Purpose of DBS

The Digital Baseline Stabilizer, DBS, tracks and corrects the baseline. The baseline refers to the zero-level for pulse analysis. Pulses are identified and analyzed relative the baseline. Having a precise baseline simplifies the classification of pulses. With a stable baseline, threshold for classification of pulses can be set much tighter.

The small pulses we are looking for is expected to have an amplitude that is lower than the best analog DC accuracy we can achieve. Hence, the analog offset is analyzed by DBS. Digital compensation then adjusts the baseline with high precision.

DBS also reduces interleaving pattern noise for interleaved digitizers. Interleaving pattern noise originates in different analog offset from different ADC cores in the interleaved ADC. The DBS identifies these differences and correct for them.

Figure 6 shows a zoom in on typical offset present on low-gain and high-gain branches. Even if the digitizer has a good DC accuracy, the offset can clearly be visible in precision 12 bits digitizers. Also, any DC contributions from the signal source in a real system can be adding to the analog offset.

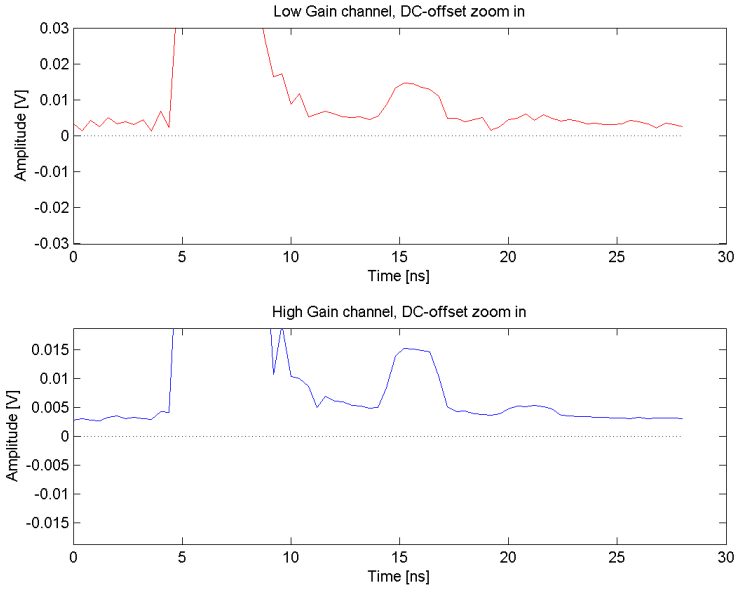

Figure 6 Zoom in on the baseline with analog offset for the respective channels. DBS is not used.

Applying DBS, the analog offset is compensated for and the baseline is forced to the target level, in this case 0. DBS corrects both for offset in the ADQ digitizer and in any external signal source. Figure 7 shows a zoom in on the baseline after correction.

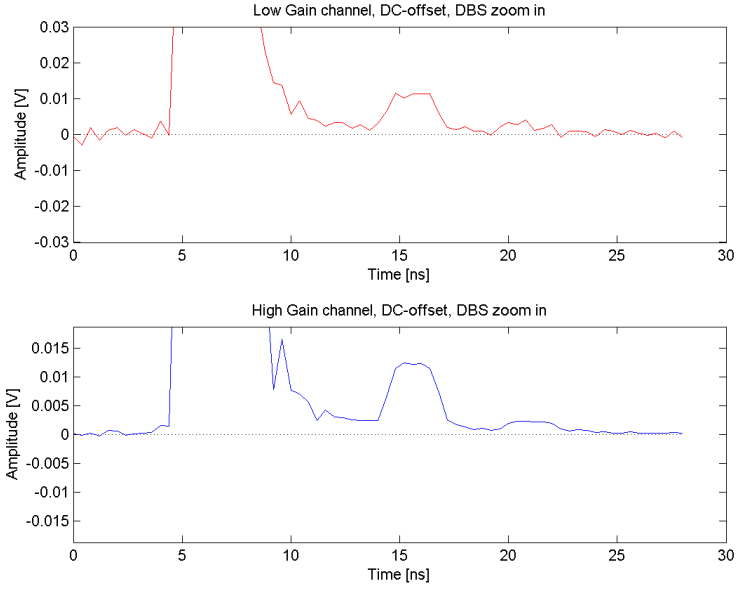

Figure 7 Zoom in on baseline corrected by DBS.

4.2 DBS principle of operation

The principle of operation is:

- Identify samples that belong to the baseline
- Compute the offset relative a user-defiend target level (and interleaving mismatch if applicable)
- Subtract the offset from all samples to set the baseline to the target level.
    - The target level is user-defined.
    - The target level is preferably set at the same level as the user-defined DC-offset.

In the example of Figure 7, the digital target value is 0 and corresponds to 0 V. We now have a solid reference point for analyzing the pulses, for example, computing energy (~area) and amplitude (~height).

It is recommended to set DBS to the same level as the DC-offset. Note that the code range is the same regardless of the analog input range.

Note that changing DC-offset changes the conditions for DBS since the baseline shifts. The DBS is, by its nature, slowly tracking the baseline and may have trouble following a changed DC-offset. Hence, it is recommended to set the DC-offset first, then wait before activating the DBS, Figure 8.

```
# Setup parameters to activate DC-offset
parameters.afe.channel[0].dc_offset = analog_offset_HG
parameters.afe.channel[1].dc_offset = analog_offset_LG
# Setup parameters to set-up DBS, but turn DBS off
parameters.signal_processing.dbs.channel[0].enabled = 0
parameters.signal_processing.dbs.channel[1].enabled = 0
parameters.signal_processing.dbs.channel[0].level = digital_offset
parameters.signal_processing.dbs.channel[1].level = digital_offset
# Set parameters to ADQ3 HW
dev.SetParameters(parameters)
time.sleep(0.1)
# Setup parameters to set-up DBS, but turn DBS off
parameters.signal_processing.dbs.channel[0].enabled = 1
parameters.signal_processing.dbs.channel[1].enabled = 1
# Set parameters to ADQ3 HW to turn on DBS
dev.SetParameters(parameters)
```

Figure 8 Python code sequence to start DBS

4.3 DBS example

Preferably, the target code level is the same as the user-defined DC-offset. In the example in Figure 4, high-gain channel is -50mV / 125mV * 2^16 = -26214. For the low-gain it is -400mV / 1000mV * 2^16 = -26214. It is recommended to set up the system so that these values are the same.

5 DBS AND DC-OFFSET INTEROPERABILITY

It is recommended so set the DC-offset before turning on DBS. It is strictly not necessary for an ordinary use-case, but it is more reliable to do that way.

Here we study how these two functions interact with each other. In the upper half of Figure 9 we can see the activation of the DC-offset. The DC-offset of -400mV is applied at time 0. The settling time is in the range of 25ms (milliseconds). In the lower half of Figure 9, the DBS is activated before the DC-offset is changed. The tracking is illustrated in the lower half.

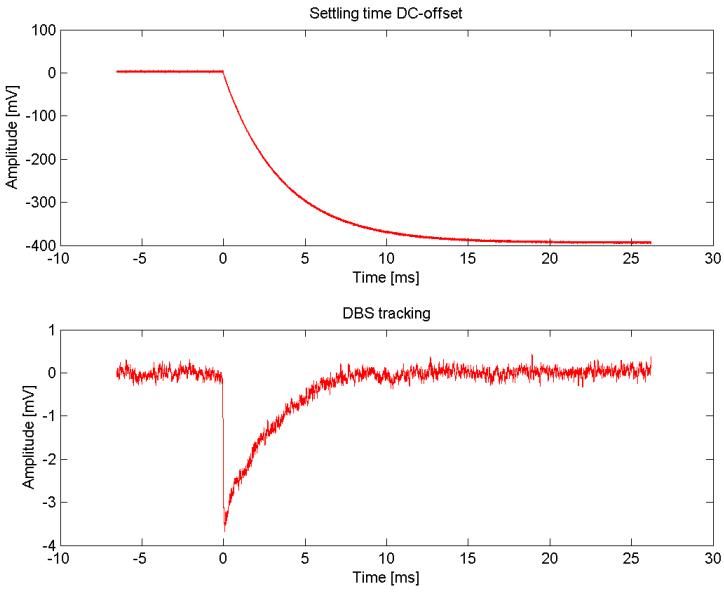

Figure 9 DC-offset settling time and DBS tracking

In this case, it works to change the DC-offset after DBS has been activated, but it is anyway recommended to apply them in the other order. It is done int this way here to be able to illustrate the effect of DBS.

6 CHANNEL COMBINER

The channel combination selects the best channel for each sample. This means in practice that the high-gain with less noise is default, but if there is an overrange in the high-gain channel, the low-gain is selected. The selection is done per sample.

The channel combiner needs the gain ratio and the baseline to scale the channels relative to each other. The design of the PDRX dual-gain amplifier sets the gain ratio. Nominal value for the built-in dual-gain amplifier is 8, but a calibration result in a value close to 8. A custom dual-gain amplifier can have a gain ratio 1 to 32.

The baseline of the channel combiner is best set to the same value as DBS. The digital code is entered.

Before the combination, the two channels are as in Figure 10.

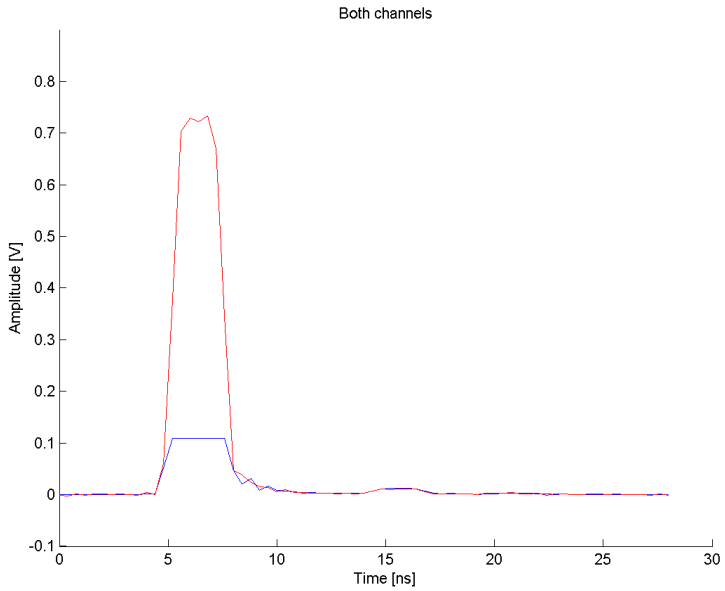

Figure 10 Both channels before combination

The combination selects the low-gain (red) when the high-gain (blue) is saturated. The combined data is drawn as black in Figure 11.

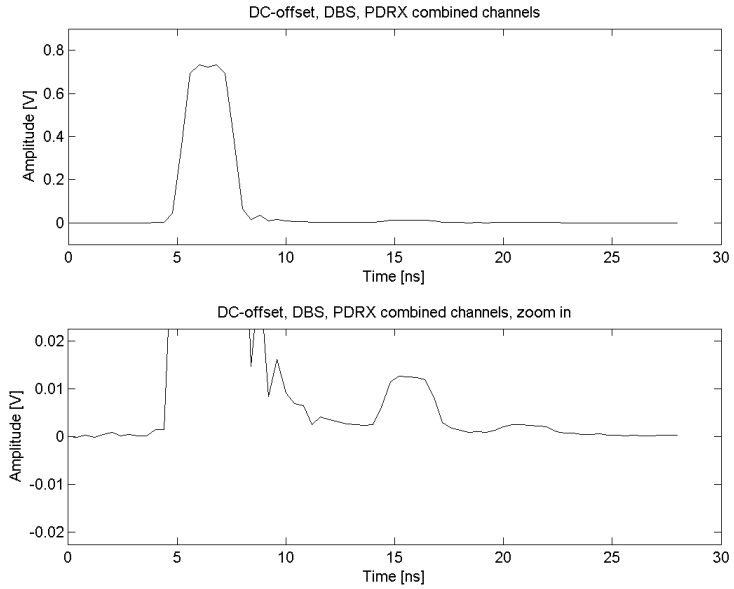

Figure 11 Combined high-gain and low-gain channels. Full scale signal and zoom in on small pulses are plotted.

The result of the channel combination can be visualized by comparing to the raw data from high-gain and low-gain. In the upper half of Figure 12 we see that the high-gain channel (blue) is cut by overrange for the large pulse. In the lower half we see that the low-gain channel (red) is nosier than

the combined data (black). The optimal combination of the two channels result in a very high dynamic range.

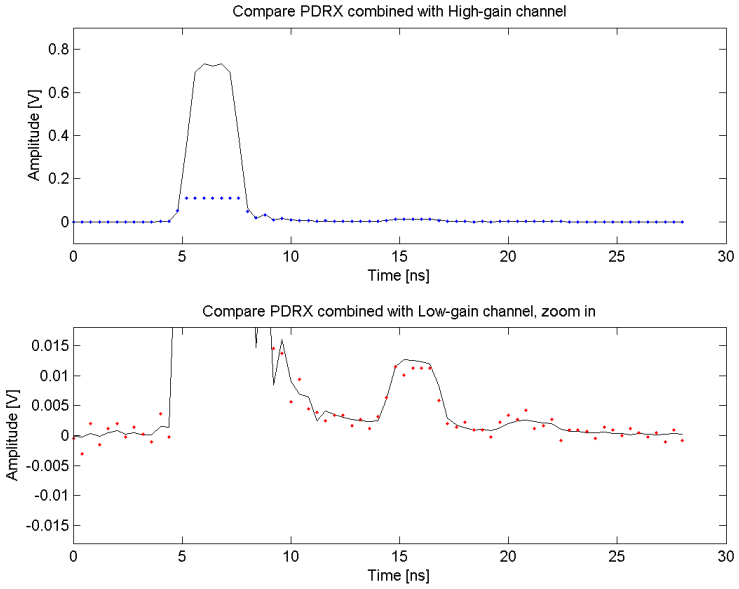

Figure 12 Compare combined data with raw data. Black lines are combined data. The blue dots are the sample points from high-gain channel. Red dots are the sample points from the low-gain channel.

The channel combination is activated by enabling the function, Figure 13. The channel combination requires a setting of a parameter named DC-offset[3], which is the common DC level for aligning the high and low gain branches and gain for setting the ratio between them.

```
# Setup PDRX parameters
parameters.signal_processing.pdrx.channel[1].enabled = 1
parameters.signal_processing.pdrx.channel[1].gain = 8
parameters.signal_processing.pdrx.channel[1].dc_offset = DIGITAL_OFFSET
```

Figure 13 Setting up the channel combination

7 RESULT OF ADQ32-PDRX DUAL-GAIN

The result by applying the features of ADQ32-PDRX, dual-gain amplifier, DC-offset, DBS, and channel combination, is that the dynamic range is increased. Table 1 is from the datasheet of ADQ32-PDRX (document number 22-2797-D). The table illustrates the difference between ADQ32 and ADQ32-PDRX and emphasizes the net gain of ADQ32-PDRX for pulse applications.

- The RMS noise level is the measured noise with terminated input. This is thus the noise generated by the digitizer. The level of the noise is set by the analog front-end configuration

[3] This is not the same parameter as the analog input or DBS. Each block has its individual baseline. It is recommended to use the same baseline is all blocks. Hence, set the DC-offset to the same value as the target value in DBS.

as well as the ADC component. The high-gain channel has a low noise floor, and hence, the ADQ32-PDRX noise level is as low as 96uV RMS. The ADQ32 has a different front-end configuration to get a different signal range and has thus 244uV RMS noise.

- The input range is the maximum allowed signal range. The range is increased from 0.5Vpp to 1Vpp in the low-gain channel of ADQ32-PDRX.
- The dynamic range in this table compare noise floor with terminated input to a theoretical sine wave at maximum input range. It is a computed value for comparing the products and not according to an established measurement standard[4]. With this measurement method, ADQ32-PDRX has 14 dB better dynamic range than ADQ32.
- The ENOB is computed form dynamic range as *(dynamic_range – 1.76)/6.02*.

Table 1 Comparison of ADQ32-PDRX to ADQ32

Parameter	Condition	ADQ32	ADQ32-PDRX	Unit
RMS noise	Terminated input	244	96	µV
Max input range		0.5	1	Vpp
DC-offset		-0.25 to 0.25	-0.5 to 0.5	V
Dynamic range		57.2	71.3	dB
ENOB		9.2	11.6	bits
Bandwidth	-3dBFS	1000	760	MHz
Attenuation at 1GHz		3	5.1	dB

8 NEGATIVE PULSES

All the discussions above is also valid for negative pulses.

For negative pulses the DC-offset is set to a positive value and the digital offset for DBS and PDRX channel combiner is set to positive values.

In this example is a negative pulse with DC-offset set to +50 mV and +400mV on the respective high-gain and low-gain channels. The digital DC level is set to +26214 in DBS and channel combiner.

[4] IEEE 1057 is an established method for characterizing data acquisition systems. The standard assumes stationary sine waves. The ADQ3-PDRX is not intended for use with stationary signals, only pulses. Hence the performance according to this standard is not relevant.

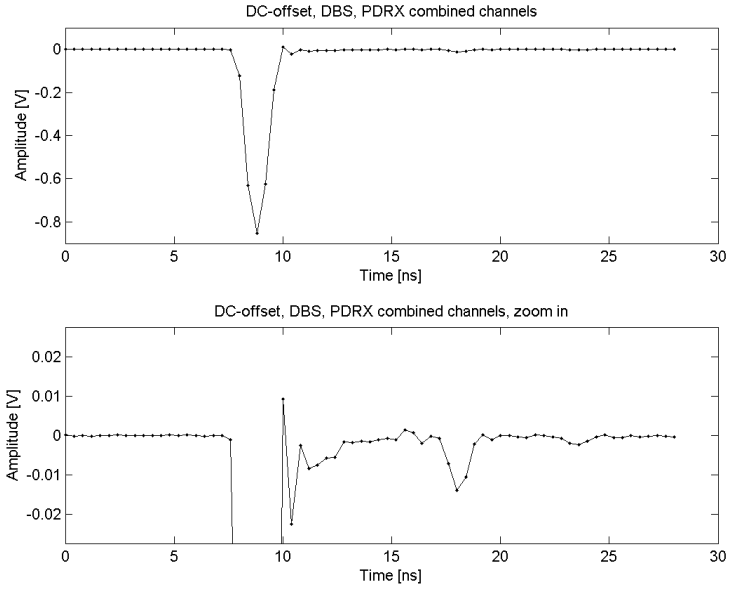

Figure 14 Negative pulses of 1.3 ns width. Full range of combined channels and zoom in on small pulse are shown.

9 FURTHER SIGNAL ANALYSIS

The features described here (dual-gain, DC-offset, DBS and PDRX channel combination) are available in the standard firmware FWDAQ. The features are also included with firmware options for averaging and pulse analysis.

9.1 Averaging using FWATD

Use the averaging firmware FWATD to accumulate waveforms of repetitive measurements to see deep in the noise floor.

9.2 Pulse analysis using FWPD

Use the firmware option FWPD to detect and analyze the pulses.

10 CHANNEL COMBINATION CHARACTERIZATION

10.1 Overview

The datasheet contains two measurements which are specific for dual-gain implementations: timing between the branches and pulse linearity in the cross-over between the branches. These effects are further described here.

10.2 Channel combination timing

The timing of the branches is not identical. This is a natural effect of electrical paths. Figure 15 illustrate the effect of a timing variation Δt between the branches. This deviation has to be kept under control since it is related to timing of the pulse.

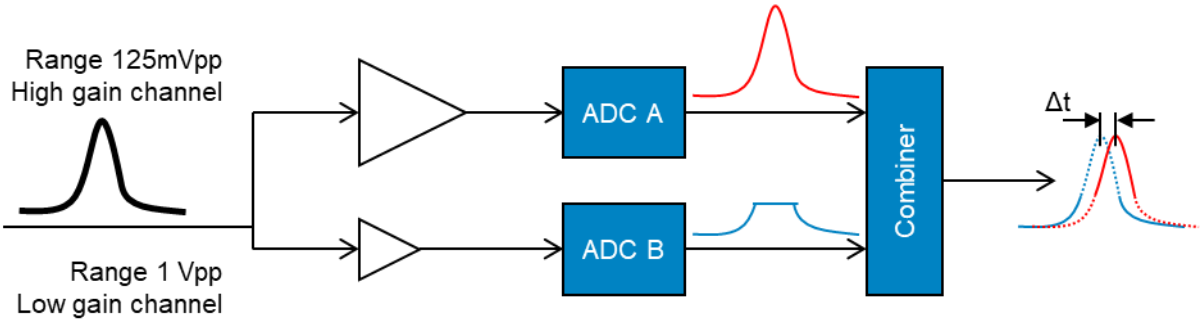

Figure 15 Timing between high-gain and low-gain channels

It is challenging to get accurate timing analysis from pulses, so the evaluation is done with a set of sine waves. With sine waves it is also easy to limit the effect of noise through curve-fitting and get accurate measurements. By sweeping the frequency, it is possible to see that the timing difference is constant over the frequency range and thus do not distort the pulse shape. The result is in the datasheet of the product. For ADQ32-PDRX it is specified to less than 13 ps over temperature and frequency[5].

10.3 Pulse amplitude linearity for combined channels

The ideal transfer function is a linear transformation from the analog input pulse amplitude to the digital output pulse amplitude. The method use is to compare the dual-gain implementation with the standard ADQ32. This method illustrates the effect of adding dual-gain amplifier. The measurement set-up is in Figure 16. A series of pulses is sent through a splitter to an ADQ32-PDRX, the device under test (DUT) and a reference in form of ADQ32.

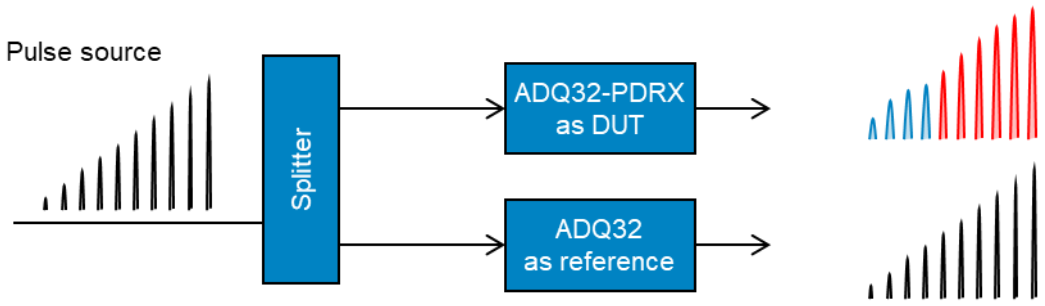

Figure 16 Measurement set-up for pulse amplitude linearity

[5] This value was valid for ADQ32-PDRX datasheet 23-2797-D. Please see spdevices.com for the latest revision of datasheet.

The pulse amplitude for the DUT is compared with the reference to get a measure of linearity as in Figure 17. The values in the datasheet are calculated and referred to the signal level and to the maximum amplitude as
(*DUT_amplitude – ref_amplitude) / ref_amplitude* and
(DUT_amplitude – ref_amplitude) / max_amplitude respectively.

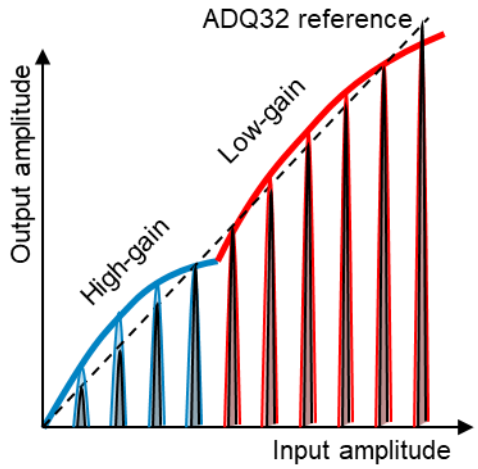

Figure 17 Illustration of how the pulse amplitude accuracy (linearity) is measured.

See datasheet for result of the linearity measurement.

11 TEST SIGNAL GENERATION

11.1 Generation of multiple pulses

The test signal in this application note is a pulse that is split into two branches and combined again with different amplitude, Figure 18. In this way a large and two small pulse are placed close to each other for illustration of the functions in ADQ3-PDRX.

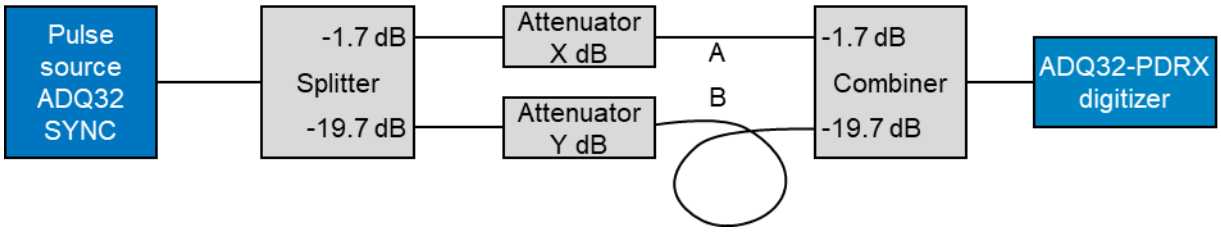

Figure 18 Pulse generation for positive polarity pulses

The pulse from the source circulates through the passive splitter network to generate three pulses, Figure 19.

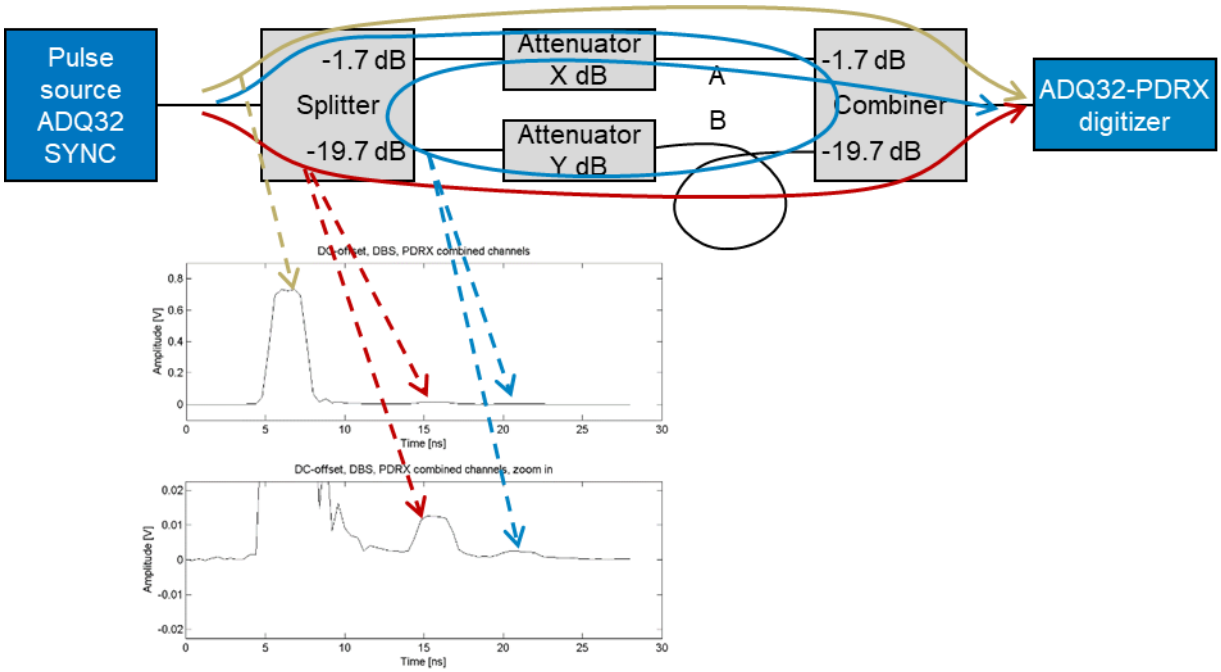

Figure 19 Test signal generation for application note.

This distribution network contains details

- The relative pulse levels are set by the attenuators X and Y.
- The splitter/combiner is asymmetrical to allow for higher power to be passed during overrange tests.
    - The minimum attenuation is 3.4dB.
    - The difference between the branches from the splitter/combiner is 36 dB
- The difference in length between A and B will determine the distance between the pulses.
    - If A < B, the large pulse is first (used in this test)
    - If B < A, the small pulse is first
- The splitter/combiner is not a circulator so some signal will go back and around the loop. The X and Y attenuators inside the loop attenuates this circulating pulse.
    - For example, if X = Y = 10 dB, the circulating pulse is 10 dB below the small pulse and can be neglected in this demonstration.
    - If A < B (large pulse first) the circulating pulse will appear 2*A after the small pulse.

11.2 Source for positive test pulse generation

The positive test signals shown here are generated using the internal pattern generator and SYNC output of the ADQ32-PDRX digitizer. The width of the pulse is 3.2 ns. This width of the pulse making it clear to distinguish in the plots. Typical code for setting up the SYNC output is in Figure 20.

```
# Periodic event generator frequency in Hz
PERIODIC_EVENT_GENERATOR_FREQUENCY = 10e3
# Configure the periodic event generator
parameters.event_source.periodic.frequency =
PERIODIC_EVENT_GENERATOR_FREQUENCY

port_id = pyadq.ADQ_PORT_SYNC
parameters.function.pulse_generator[0].source =
pyadq.ADQ_EVENT_SOURCE_PERIODIC
parameters.function.pulse_generator[0].edge = pyadq.ADQ_EDGE_RISING
parameters.function.pulse_generator[0].length = 8
parameters.port[port_id].pin[0].direction=pyadq.ADQ_DIRECTION_OUT
parameters.port[port_id].pin[0].invert_output=False
parameters.port[port_id].pin[0].function=pyadq.ADQ_FUNCTION_PULSE_GENERATOR0
```

Figure 20 Setting up SYNC as test pulse

11.3 Source for negative test pulse generation

The negative pulse is generated from an HP 8131A pulse generator and sent through the same pulse splitter network, Figure 19. The pulse width is 1.3 ns. Note that this test pulse is considerably shorter than the one used for positive tests, which result in different looking pulses.

11.4 Plotting

The output data from the board with enabled channel combination is combined result on channel index 1 and high gain channel data on index 0. Converting the data to Volt and plot result in this way, Figure 21:

```
plt.figure(1)
plt.plot(record_1.data/2**16-ANALOG_OFFSET_LG/1000)
plt.ylabel('Amplitude [v]')
plt.figure(2)
plt.plot(record_0.data/2**16/8-ANALOG_OFFSET_HG/1000)
plt.ylabel('Amplitude [v]')
```

Figure 21 Plotting the result