Digital Time-Interleaved ADC Mismatch Error Correction Embedded into High-Performance Digitizers

BY PER LÖWENBORG, PH.D., DOCENT

1   TIME-INTERLEAVED ANALOG-TO-DIGITAL CONVERTERS AND MISMATCH ERRORS

Achievable resolution and spurious performance of analog-to-digital converters (ADCs) are tightly connected to the maximum sampling frequency of the device. Today, in early 2013, sampling rates of commercially available 16-bit monolithic, single-core (non-interleaved) ADCs are limited to 250 MS/s while 14-bit ADCs can be found up to 400 MS/s. The corresponding number for a single-core 12-bit ADC design is 1500 MS/s.

There are however many applications where more dense sampling grids and higher instantaneous bandwidths are needed than what can be supported with a single-core ADC with a given resolution. The remedy to this problem is spelled time-interleaving, which is a technique to increase the nominal sampling frequency by using an array of ADCs and where each ADC is clocked with a unique, phase-skewed sampling clock relative to the other ADCs. The principle of two time-interleaved ADCs is shown in Figure **1**.
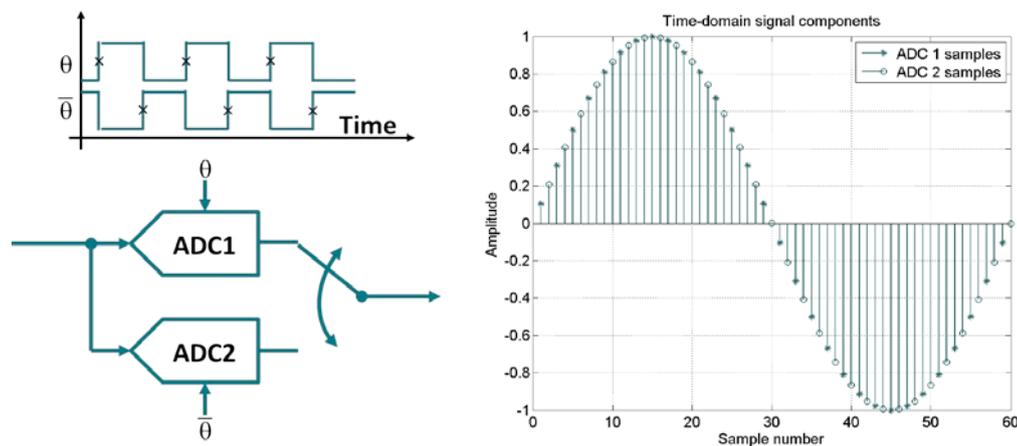
Figure 1: The principle of two time-interleaved ADCs. The two ADCs are clocked at opposite sampling clock phases, effectively producing a sampling grid which is twice as dense compared to that of one ADC. Thus, the sampling frequency is doubled and the vertical resolution is ideally the same as that of each ADC.

For resolutions of 10 bits or more, time-interleaved sampling alone is however not enough to solve the sampling frequency problem in practice, since the time-interleaving principle requires that the ADCs used are behaving identically from an input-output perspective. If not, differences in gain and phase-delay responses as well as DC offset between the ADCs in the array will create a nonlinear distortion effect called *aliasing*. The aliasing consists of new frequency components not present in the input signal and these are in fact frequency-shifted versions of the desired input signal spectrum.

The left-hand plot in Figure **2** illustrates how aliasing appears as a new frequency component as a result of a (large) gain mismatch between two ADCs. The total signal (dashed blue curve) is the composition of two components, one at the desired frequency (solid black curve) and an undesired aliased component (solid red curve) occurring at a different frequency. The right-hand plot in Figure **2** shows the corresponding amplitude spectrum. The aliasing of a two-way time-interleaved system occurs as an image of the input signal spectrum, mirrored in a quarter of the aggregate sampling frequency.

The net effect of mismatch is that it degrades the ADC effective resolution and spurious response. For resolutions of 10 bits or more, calibration and/or post-processing is necessary to remove the mismatch errors, thereby effectively emulating an array of identically-behaving ADCs with resolution preserved as that of each ADC in the array.

An example of typical measured gain and phase-delay mismatch when time-interleaving two 400 MS/s, 14-bit ADCs are shown in Figure **3**. From the figure, it is evident that the mismatch varies over frequency (labeled "Uncalibrated") and in order to compensate or remove the errors, the relative gain and phase delay cannot be compensated fully with a static (frequency-independent) gain and delay compensation. The ADX2 and ADX4 digital post-processing IP-cores from SP Devices are designed to remove such mismatch over frequency with high accuracy.
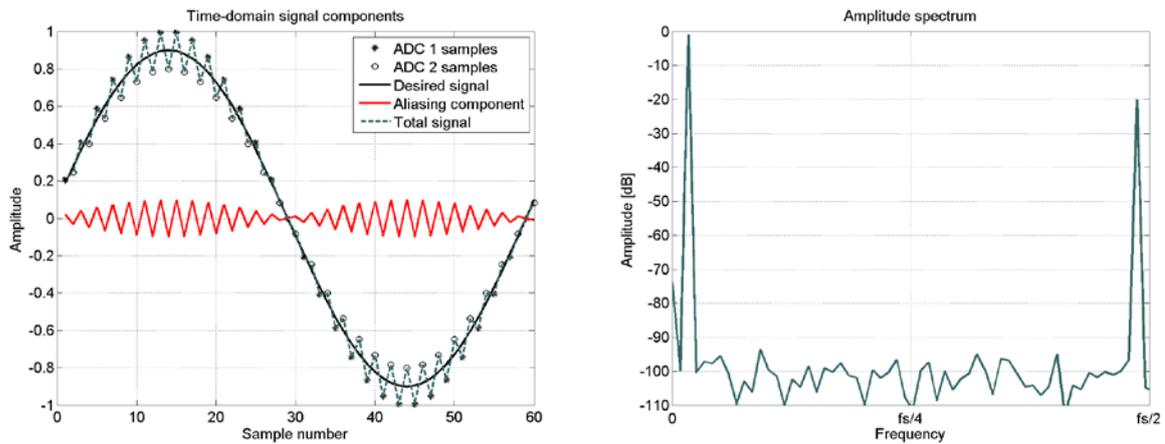
Figure 2: An illustration of aliasing as a result of gain mismatch between two time-interleaved ADCs (left). The total signal constitutes a combination of a desired signal component and an unwanted aliasing component. The resulting amplitude spectrum of the total signal containing the desired (low-frequency) signal and an aliasing component occurring as an attenuated and mirror-imaged copy of the desired (high-frequency) signal (right).
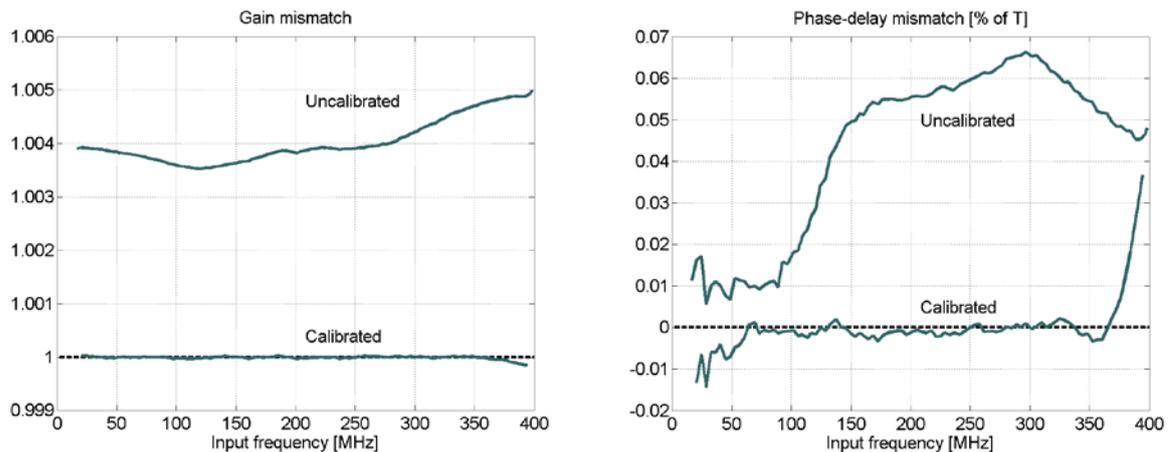
Figure 3: Measured typical relative gain and phase-delay mismatch of two discrete time-interleaved 400 MS/s, 14-bit ADCs (labeled "Uncalibrated"). The corresponding curves labeled "Calibrated" are the measured effective mismatch when using the SP Devices ADX2 digital post-processing IP-core for mismatch error correction. The measurements are made with a system sampling frequency of 800 MS/s and the instantaneous post-processing bandwidth is 360 MHz.

The resulting effective mismatch when using ADX2 is shown as the curves labeled "Calibrated" in Figure **3**.

2   RESULTS OF DIGITAL MISMATCH ERROR CORRECTION

Having reviewed the basics of time-interleaving and mismatch effects, we will now present typical mismatch errors and spurious performance measured on SP Devices' digitizers using high-performance ADCs and digital mismatch error correction. The digitizer models used and the corresponding sampling frequency, resolution, ADC parts, and post-processing IP-cores are listed in Table 1.

Table 1: Overview of selected digitizers, ADCs, and embedded IP-core for time-interleaved ADC mismatch error correction.

Digitizer Model	Sampling Frequency [MS/s]	Resolution [Bits]	ADC Part	IP-Core for Mismatch Error Correction
ADQ114	800	14	ADS5474	ADX2
ADQ1600	1600	14	ADS5474	ADX4
ADQ412-3G	3600	12	ADC12D1800	ADX4

PXIe versions of the digitizers used for gathering the measured post-processing enhancement results are shown in Figure **4**.

Figure 4: Three digitizer product models of SP Devices. To the left, an ADQ114 in a PXIe format. The single analog input is sampled at 800 MS/s and the resolution is 14 bits. This is enabled by two time-interleaved Texas Instruments ADS5474 ADCs and an embedded real-time implementation of the mismatch error correction IP-core ADX2 from SP Devices.

In the middle, an ADQ1600 in a PXIe format. The single analog input is sampled at 1600 MS/s. This is achieved by four time-interleaved Texas Instruments ADS5474 ADCs and an embedded real-time implementation of the mismatch error correction IP-core ADX4 from SP Devices.

To the right, an ADQ412 digitizer in a PXIe form factor. When operated in dual-input mode, the two analog input channels are each sampled at 3600 MS/s. This is enabled by the Texas Instruments ADC12D1800 ADCs configured in so called DES-MODE and a dual embedded real-time implementation of the mismatch error correction IP-core ADX4 from SP Devices.

In Figure **5** to Figure **8**, example amplitude spectra for single-tone and two-tone tests are shown for each digitizer model and the respective IP-core together with peak aliasing distortion level and offset mismatch measured over a complete Nyquist frequency band. Definitions of spectrum plot markers are given in Table 2.

For each digitizer model, a separated two-tone test is shown which gives a clear indication of that the time-interleaved mismatch error correction (ADX IP-core family) is indeed wideband and is compensating the errors over frequency. Static (frequency-independent) correction often fails for such tests since whereas gain and sampling time can be adjusted for each frequency independently using a static approach, it cannot compensate frequency-dependent errors which are likely to be present (and different) at two widely separated frequencies.

For the models ADQ114 and ADQ1600 in Figure **5** to Figure **7** respectively, which employ discrete ADCs, the raw matching performance gives an SFDR of about 40 dBc which is set by the combined gain and phase-delay mismatch. For the ADQ412-3G in Figure **8** which uses an ADC with fully-integrated time-interleaved ADCs, the SFDR which is also here limited by gain and phase-delay mismatch between the ADC core is about 20 dB better than the previous cases, i.e. 60 dBc. From the number of aliasing tones, their frequency location, and relative strengths, one can also notice from Figure **8** a) to d) that the ADC12D1800 ADC produces aliasing distortion that occurs when time-interleaving four or more ADCs. Thus it can benefit from using four-way time-interleaved ADC mismatch error correction like the ADX4.

The real-time processing of the digital post-processing IP-cores (FPGA implementations) enhances the SFDR of all three models over 90% of the aggregate system first Nyquist frequency band. The suppression of aliasing distortion due to time-interleaved ADC mismatch then occurs in a "correction frequency band" having a low-pass character (see Figure **5**e). For the model ADQ114, which has an analog input bandwidth exceeding two Nyquist frequency bands, operation in the second Nyquist frequency band is supported. For Nyquist frequency bands above the first, the correction frequency band has a band-pass character (see Figure **6**e).

The ADX2 and ADX4 IP-cores can from Figure **5** and Figure **7** be seen to provide up to 45 dB improvements for the digitizers using discrete time-interleaved 14-bit ADCs, reducing the aliasing distortion tones down to the mid-eighties or better. Figure **8** shows a corresponding improvement down to about 77 dBFs for the 12-bit ADQ412-3G digitizer. The final SFDR performance levels of some 85 and 77 dB are what are typically expected for a single-core 14-bit and 12-bit ADC, respectively and it is mainly noise and static nonlinearity that sets a bound on the improvement. Thus, one can draw the conclusion that *the digital time-interleaved ADC mismatch error correction IP-cores, ADX2 and ADX4, make the SFDR-performance of the time-interleaved ADC array to correspond to that of a single-core ADC*. This is true both for solutions using discrete time-interleaved ADCs as well as singe-die ADC implementations.

Table 2: Definition of spectrum plot markers in Figure **5** to Figure **8**.

Marker	Error Type
SIG	Fundamental tone
DC	DC level
TISig	Aliasing tone due to ADC gain and phase-delay mismatch
TIDC	Spurious tone due to ADC offset mismatch
HD2	Second-order nonlinear harmonic distortion tone
HD3	Third-order nonlinear harmonic distortion tone
IM2	Second-order nonlinear intermodulation distortion tone
IM3	Third-order nonlinear intermodulation distortion tone
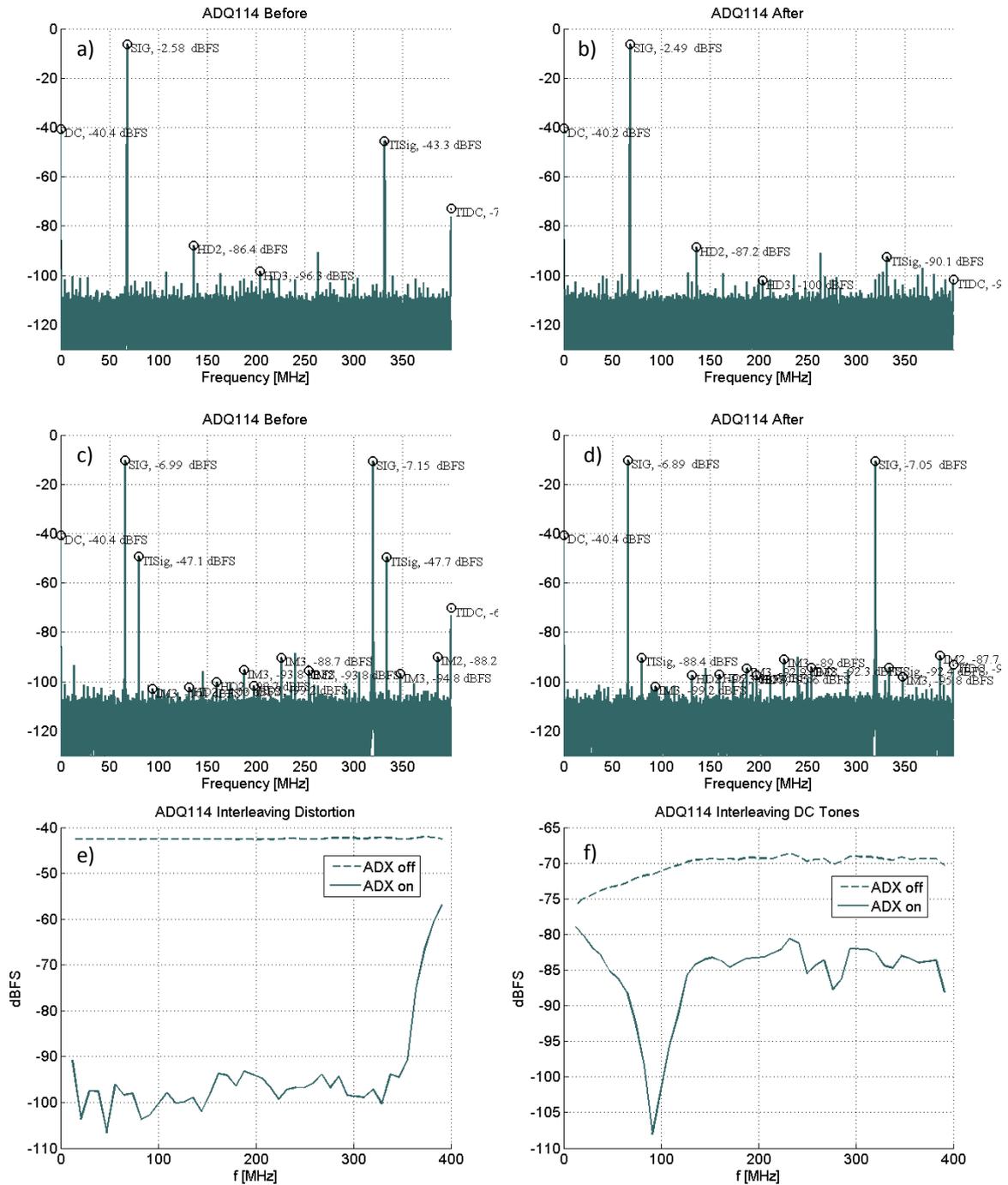
Figure 5: Measured performance of two time-interleaved ADS5474 ADCs and the digital time-interleaved ADC mismatch error correction IP-core ADX2. The measurements are taken from the SP Devices standard digitizer product ADQ114 for frequencies in the first system Nyquist frequency band.

An example single-tone amplitude spectrum with ADX2 bypassed (a). An example single-tone amplitude spectrum with ADX2 active (b). An example two-tone amplitude spectrum with ADX2 bypassed (c). An example two-tone amplitude spectrum with ADX2 active (d). Peak aliasing level with a bypassed and an active IP-core for frequencies (e). Peak offset mismatch spurious tone level with a bypassed and an active IP-core (f).
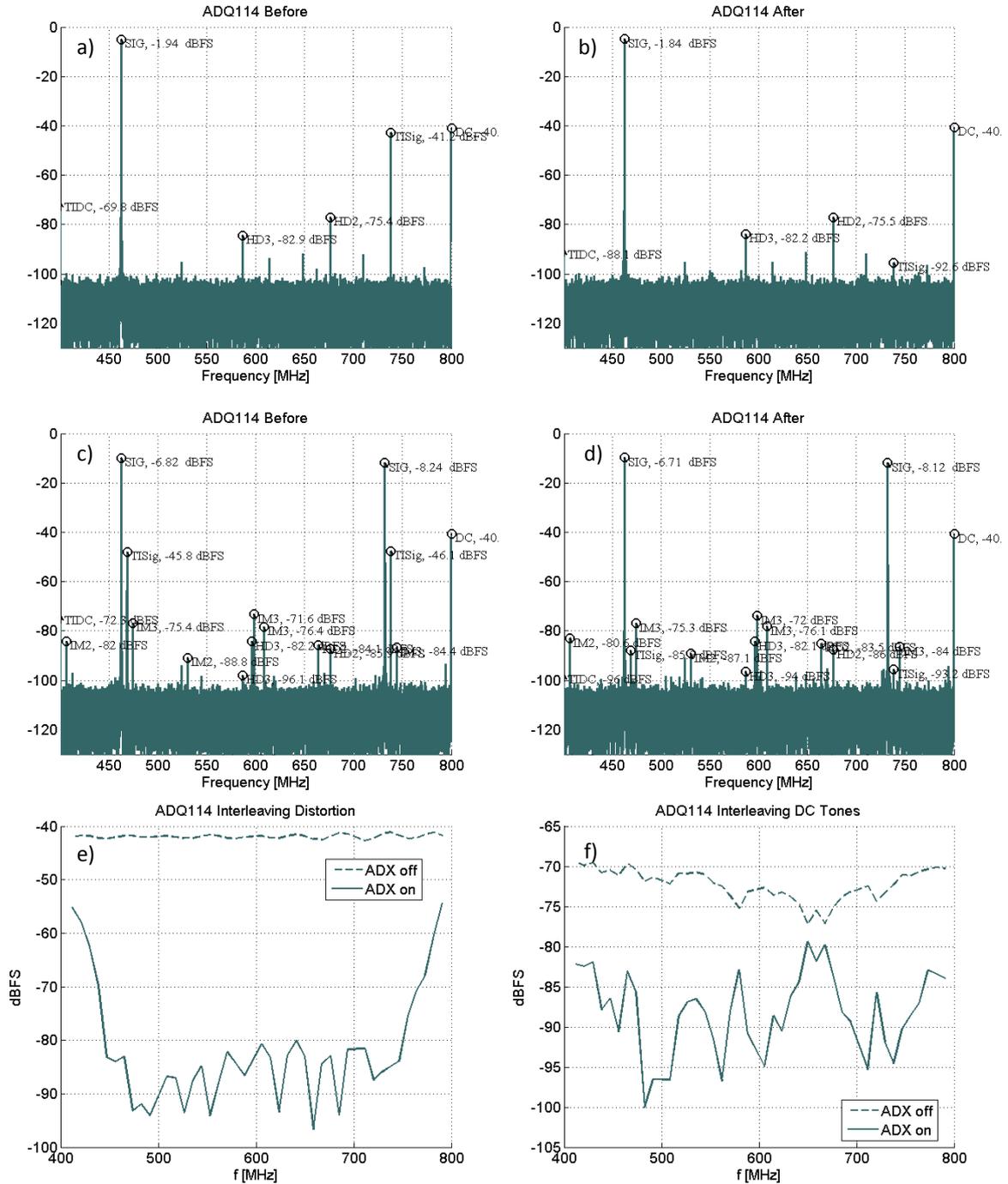
Figure 6: Measured performance of two time-interleaved ADS5474 ADCs and the digital time-interleaved ADC mismatch error correction IP-core ADX2. The measurements are taken from the SP Devices standard digitizer product ADQ114 for frequencies in the second system Nyquist frequency band.

An example single-tone amplitude spectrum with ADX2 bypassed (a). An example single-tone amplitude spectrum with ADX2 active (b). An example two-tone amplitude spectrum with ADX2 bypassed (c). An example two-tone amplitude spectrum with ADX2 active (d). Peak aliasing level with a bypassed and an active IP-core for frequencies (e). Peak offset mismatch spurious tone level with a bypassed and an active IP-core (f).
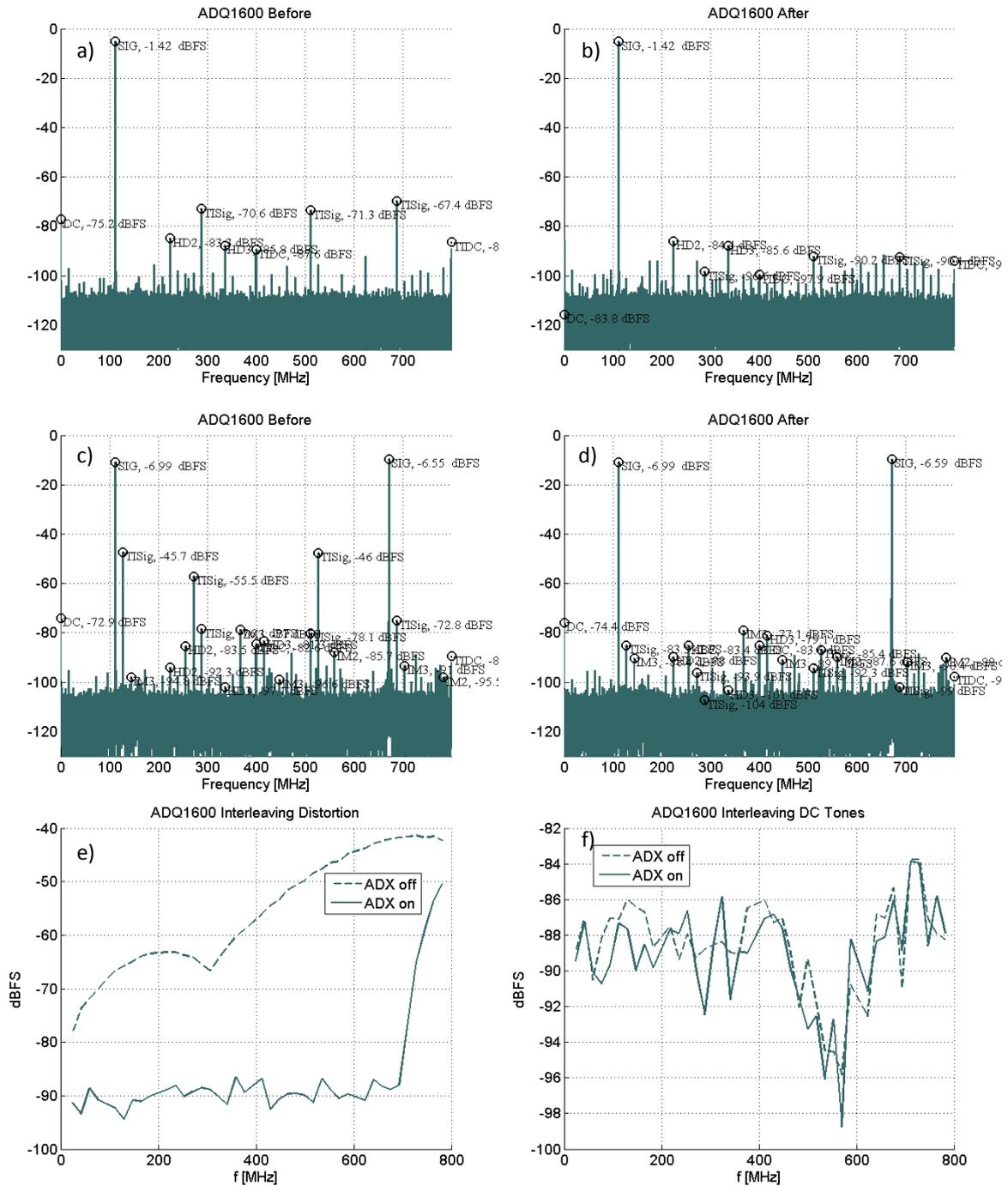
Figure 7: Measured performance of four time-interleaved ADS5474 ADCs and the digital time-interleaved ADC mismatch error correction IP-core ADX4. The measurements were taken from the SP Devices standard digitizer product ADQ1600.

An example single-tone amplitude spectrum with ADX4 bypassed (a). An example single-tone amplitude spectrum with ADX4 active (b). An example two-tone amplitude spectrum with ADX4 bypassed (c). An example two-tone amplitude spectrum with ADX4 active (d). Peak mismatch-induced aliasing level with a bypassed and an active IP-core for frequencies (e). Peak offset mismatch spurious tone level with a bypassed and an active IP-core (f).
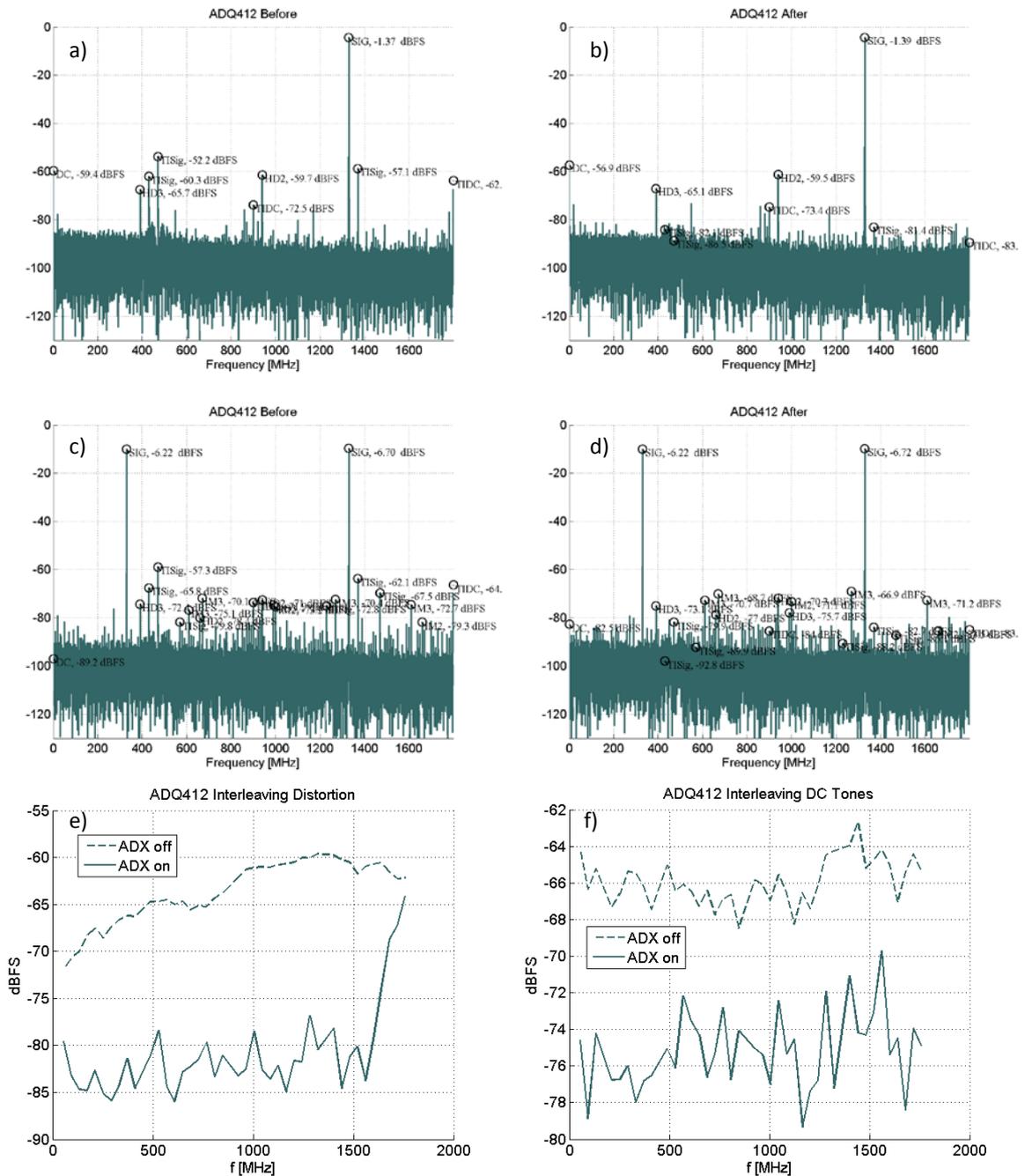
Figure 8: Measured performance of an ADC12D1800 ADC and the digital time-interleaved ADC mismatch error correction IP-core ADX4. The measurements were taken from the SP Devices standard digitizer product ADQ412 -3G.

An example single-tone amplitude spectrum with ADX4 bypassed (a). An example single-tone amplitude spectrum with ADX4 active (b). An example two-tone amplitude spectrum with ADX4 bypassed (c). An example two-tone amplitude spectrum with ADX4 active (d). Peak mismatch-induced aliasing level with a bypassed and an active IP-core for frequencies (e). Peak offset mismatch spurious tone level with a bypassed and an active IP-core (f).